

# NCP6151S/NCP6131S

## Preliminary Datasheet

### Dual Output 3/4 Phase +1/0 Phase Controller with single SVID Interface for Desktop and Notebook CPU Applications

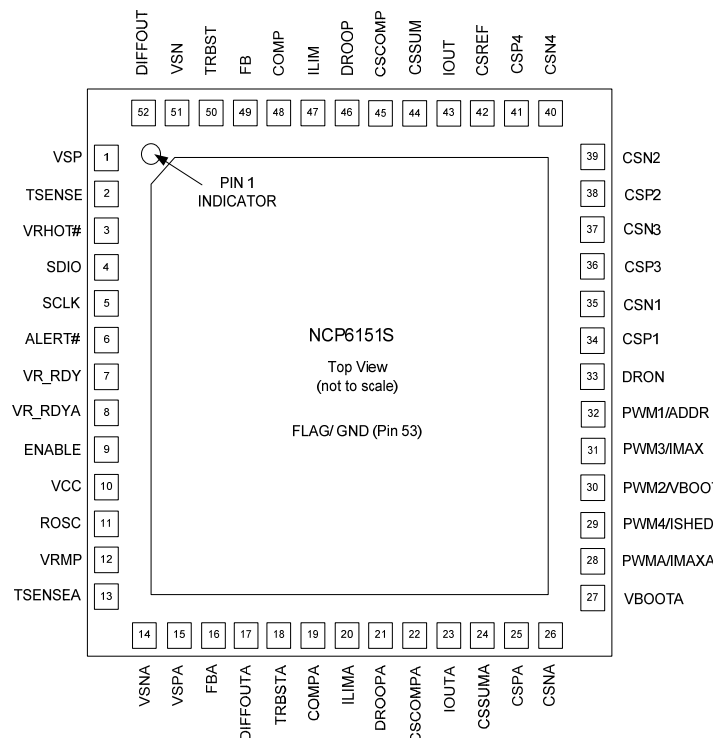


ON Semiconductor

The NCP6151S/NCP6131S dual output four plus one phase buck solution is optimized for Intel VR12 compatible CPUs. The controller combines true differential voltage sensing, differential inductor DCR current sensing, input voltage feed-forward, and adaptive voltage positioning to provide accurately regulated power for both Desktop and Notebook applications. The control system is based on Dual-Edge pulse-width modulation (PWM) combined with DCR current sensing providing the fastest initial response to dynamic load events and reduced system cost. It also sheds to single phase during light load operation and can auto frequency scale in light load while maintaining excellent transient performance. Dual high performance operational error amplifiers are provided to simplify compensation of the system. Patented Dynamic Reference Injection further simplifies loop compensation by eliminating the need to compromise between closed-loop transient response and Dynamic VID performance. Patented Total Current Summing provides highly accurate current monitoring for droop and digital current monitoring.

#### Features

- Meets Intel VR12/IMVP7 Specifications
- Current Mode Dual Edge Modulation for Fastest Initial Response to Transient Loading
- Dual High Performance Operational Error Amplifier
- One Digital Soft Start Ramp for Both Rails
- Dynamic Reference Injection® (Patent #US07057381)
- Accurate Total Summing Current Amplifier(Patent #US006683441)
- DAC with Droop Feed-forward Injection(Patent Pending)
- Dual High Impedance Differential Voltage and Total Current Sense Amplifiers
- Phase-to-Phase Dynamic Current Balancing
- "Lossless" DCR Current Sensing for Current Balancing
- Summed Thermally Compensated Inductor Current Sensing for Droop
- True Differential Current Balancing Sense Amplifiers for Each Phase
- Adaptive Voltage Positioning (AVP)
- Switching Frequency Range of 100KHz – 1.0MHz
- Startup into Pre-Charged Loads While Avoiding False OVP



(QFN52 Single Row Pin Package Shown)

| Device          | Package          | Shipping         |
|-----------------|------------------|------------------|
| NCP6151S52MNR2G | QFN52 Single Row | 2500/Tape & Reel |
| NCP6131S52MNR2G | QFN52 Single Row | 2500/Tape & Reel |

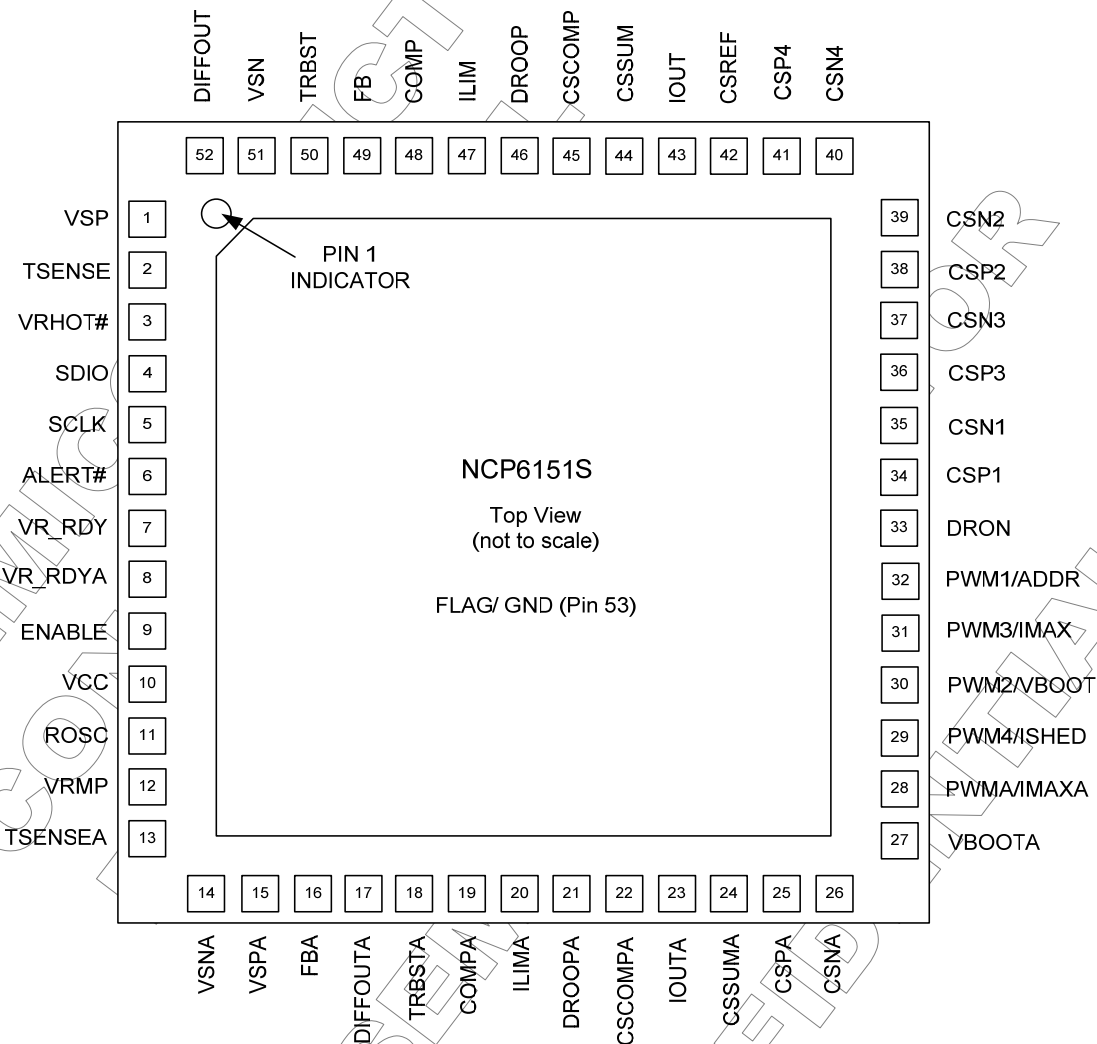
Pb-free and Halide-free packages are available

- Power Saving Phase Shedding
- Vin Feed Forward Ramp Slope
- Pin Programming for Internal SVID parameters
- Over Voltage Protection (OVP) & Under Voltage Protection (UVP)
- Over Current Protection (OCP)
- Dual Power Good Output with Internal Delays

#### Applications

- Desktop & Notebook Processors

**To Be Modified**

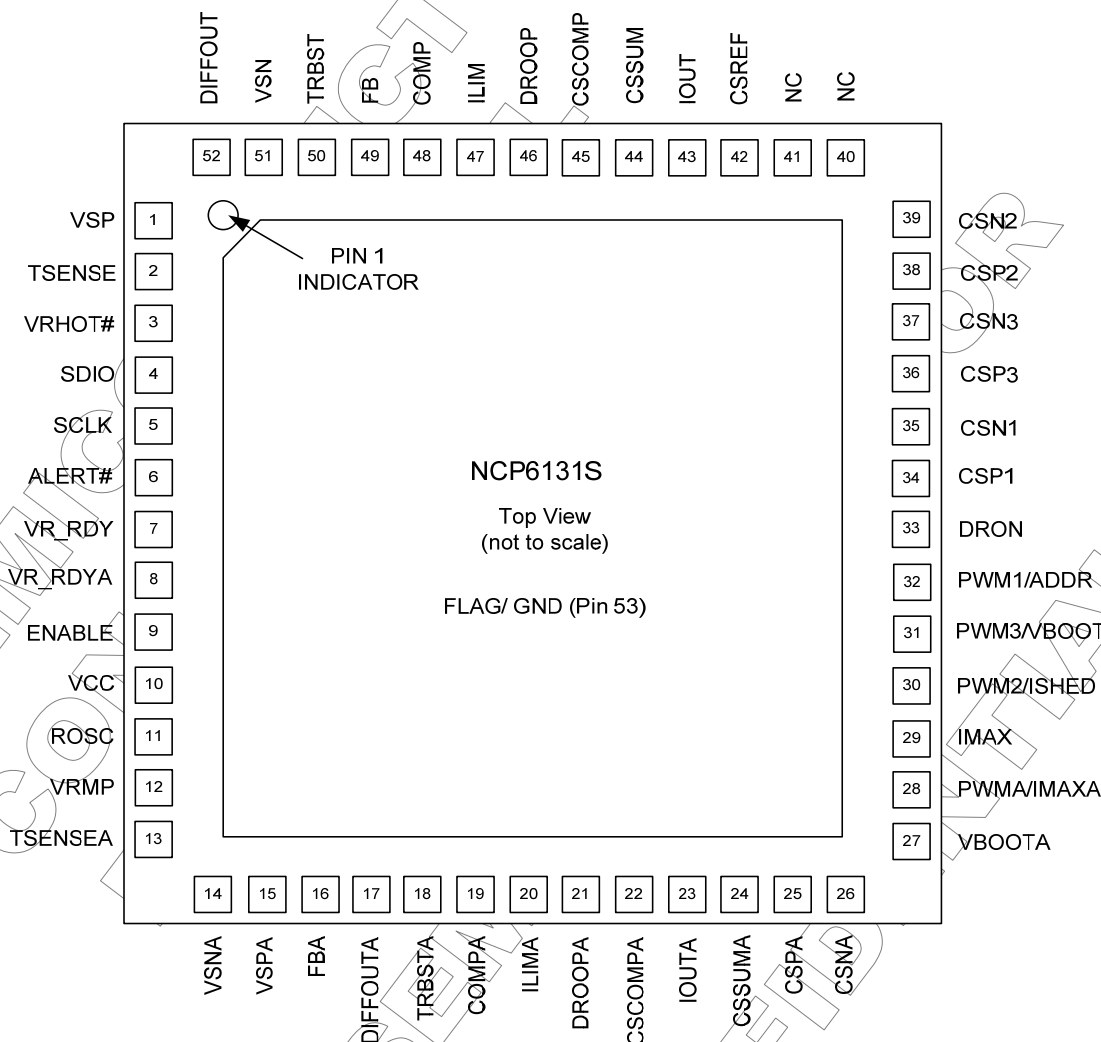


**NCP6151S QFN52 Single Row Pin List and Descriptions**

| Pin No. | Symbol  | Description                                                                                |
|---------|---------|--------------------------------------------------------------------------------------------|
| 1       | VSP     | Non-inverting input to the core differential remote sense amplifier.                       |
| 2       | TSENSE  | Temp Sense input for the multiphase converter                                              |
| 3       | VR_HOT# | Thermal logic output for over temperature.                                                 |
| 4       | SDIO    | Serial VID data interface.                                                                 |
| 5       | SCLK    | Serial VID clock.                                                                          |
| 6       | ALERT#  | Serial VID ALERT#.                                                                         |
| 7       | VR_RDY  | Open drain output. High indicates that the core output is regulating.                      |
| 8       | VR_RDYA | Open drain output. High indicates that the aux output is regulating.                       |
| 9       | ENABLE  | Logic input. Logic high enables both outputs and logic low disables both outputs.          |
| 10      | VCC     | Power for the internal control circuits. A decoupling capacitor is connected from this pin |

|    |                    |                                                                                                                                                             |
|----|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    |                    | to ground.                                                                                                                                                  |
| 11 | ROSC               | A resistance from this pin to ground programs the oscillator frequency. This pin supplies a trimmed output voltage of 2V.                                   |
| 12 | VRMP               | Feed-forward input of Vin for the ramp slope compensation. The current fed into this pin is used to control the ramp of PWM slope                           |
| 13 | TSENSEA            | Temp Sense input for the single phase converter                                                                                                             |
| 14 | VSNA               | Inverting input to the aux differential remote sense amplifier                                                                                              |
| 15 | VSPA               | Non-inverting input to the aux differential remote sense amplifier                                                                                          |
| 16 | FBA                | Error amplifier voltage feedback for aux output                                                                                                             |
| 17 | DIFFOUTA           | Output of the aux differential remote sense amplifier                                                                                                       |
| 18 | TRBSTA             | Compensation pin for aux rail load transient boost.                                                                                                         |
| 19 | COMPA              | Output of the aux error amplifier and the inverting input of the PWM comparator for aux output                                                              |
| 20 | ILIMA              | Over current shutdown threshold setting for aux output. A resistor to CSCOMPA sets the threshold.                                                           |
| 21 | DROOPA             | Used to program droop function for aux output. It's connected to the resistor divider placed between CSCOMPA and CSREFA.                                    |
| 22 | CSCOMPA            | Output of total current sense amplifier for aux output                                                                                                      |
| 23 | IOUTA              | Total output current monitor for aux output                                                                                                                 |
| 24 | CSSUMA             | Inverting input of total current sense amplifier for aux output                                                                                             |
| 25 | CSPA               | Non-Inverting input to aux current sense amplifier                                                                                                          |
| 26 | CSNA               | Inverting input to aux current sense amplifier                                                                                                              |
| 27 | VBOOTA             | VBOOTA Voltage input pin. Set to adjust the aux boot-up voltage                                                                                             |
| 28 | PWMA/IMAXA         | Aux PWM output to gate driver. Also as ICC_MAXA input pin for aux rail. During start up it is used to program ICC_MAXA with a resistor to ground            |
| 29 | PWM4 (Rev 0)       | Phase 4 PWM output. Pull to Vcc will configure as 3-phase operation.                                                                                        |
|    | PWM4/ISHED (Rev 1) | Phase 4 PWM output. Also as Phase shedding Input. During start up a resistor to ground on this pin programs the ISHED voltage.                              |
| 30 | PWM2/VBOOT         | Phase 2 PWM output. Also as VBOOT input pin to adjust the core rail boot-up voltage. During start up it is used to program VBOOT with a resistor to ground. |
| 31 | PWM3/IMAX          | Phase 3 PWM output. Also as ICC_MAX Input Pin for core rail. During start up it is used to program ICC_MAX with a resistor to ground.                       |
| 32 | PWM1/ADDR          | Phase 1 PWM output. Also as Address program pin. A resistor to ground on this pin programs the SVID address of the device.                                  |
| 33 | DRON               | Bidirectional gate drive enable for core output.                                                                                                            |
| 34 | CSP1               | Non-inverting input to current balance sense amplifier for phase 1                                                                                          |
| 35 | CSN1               | Inverting input to current balance sense amplifier for phase 1                                                                                              |
| 36 | CSP3               | Non-inverting input to current balance sense amplifier for phase 3                                                                                          |
| 37 | CSN3               | Inverting input to current balance sense amplifier for phase 3                                                                                              |
| 38 | CSP2               | Non-inverting input to current balance sense amplifier for phase 2                                                                                          |
| 39 | CSN2               | Inverting input to current balance sense amplifier for phase 2                                                                                              |
| 40 | CSN4               | Inverting input to current balance sense amplifier for phase 4                                                                                              |
| 41 | CSP4               | Non-inverting input to current balance sense amplifier for phase 4                                                                                          |
| 42 | CSREF              | Total output current sense amplifier reference voltage input.                                                                                               |
| 43 | IOUT               | Total output current monitor for core output.                                                                                                               |
| 44 | CSSUM              | Inverting input of total current sense amplifier for core output.                                                                                           |
| 45 | CSCOMP             | Output of total current sense amplifier for core output.                                                                                                    |
| 46 | DROOP              | Used to program droop function for core output. It's connected to the resistor divider placed between CSCOMP and CSREF summing node.                        |
| 47 | ILIM               | Over current shutdown threshold setting for core output. Resistor to CSCOMP to set threshold.                                                               |
| 48 | COMP               | Output of the error amplifier and the inverting inputs of the PWM comparators for the core output.                                                          |
| 49 | FB                 | Error amplifier voltage feedback for core output                                                                                                            |
| 50 | TRBST              | Compensation pin for core rail load transient boost.                                                                                                        |

|    |            |                                                                  |
|----|------------|------------------------------------------------------------------|
| 51 | VSN        | Inverting input to the core differential remote sense amplifier. |
| 52 | DIFFOUT    | Output of the core differential remote sense amplifier.          |
| 53 | FLAG / GND | Power supply return ( QFN Flag )                                 |



**NCP6131S QFN52 Single Row Pin List and Descriptions**

| Pin No. | Symbol  | Description                                                                                           |
|---------|---------|-------------------------------------------------------------------------------------------------------|
| 1       | VSP     | Non-inverting input to the core differential remote sense amplifier.                                  |
| 2       | TSENSE  | Temp Sense input for the multiphase converter                                                         |
| 3       | VR_HOT# | Thermal logic output for over temperature.                                                            |
| 4       | SDIO    | Serial VID data interface.                                                                            |
| 5       | SCLK    | Serial VID clock.                                                                                     |
| 6       | ALERT#  | Serial VID ALERT#.                                                                                    |
| 7       | VR_RDY  | Open drain output. High indicates that the core output is regulating.                                 |
| 8       | VR_RDYA | Open drain output. High indicates that the aux output is regulating.                                  |
| 9       | ENABLE  | Logic input. Logic high enables both outputs and logic low disables both outputs.                     |
| 10      | VCC     | Power for the internal control circuits. A decoupling capacitor is connected from this pin to ground. |

|    |                       |                                                                                                                                                             |
|----|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11 | ROSC                  | A resistance from this pin to ground programs the oscillator frequency. This pin supplies a trimmed output voltage of 2V.                                   |
| 12 | VRMP                  | Feed-forward input of Vin for the ramp slope compensation. The current fed into this pin is used to control the ramp of PWM slope                           |
| 13 | TSENSEA               | Temp Sense input for the single phase converter                                                                                                             |
| 14 | VSNA                  | Inverting input to the aux differential remote sense amplifier                                                                                              |
| 15 | VSPA                  | Non-inverting input to the aux differential remote sense amplifier                                                                                          |
| 16 | FBA                   | Error amplifier voltage feedback for aux output                                                                                                             |
| 17 | DIFFOUTA              | Output of the aux differential remote sense amplifier                                                                                                       |
| 18 | TRBSTA                | Compensation pin for aux rail load transient boost.                                                                                                         |
| 19 | COMPA                 | Output of the aux error amplifier and the inverting input of the PWM comparator for aux output                                                              |
| 20 | ILIMA                 | Over current shutdown threshold setting for aux output. A resistor to CSCOMPA sets the threshold.                                                           |
| 21 | DROOPA                | Used to program droop function for aux output. It's connected to the resistor divider placed between CSCOMPA and CSREFA.                                    |
| 22 | CSCOMPA               | Output of total current sense amplifier for aux output                                                                                                      |
| 23 | IOUTA                 | Total output current monitor for aux output                                                                                                                 |
| 24 | CSSUMA                | Inverting input of total current sense amplifier for aux output                                                                                             |
| 25 | CSPA                  | Non-Inverting input to aux current sense amplifier                                                                                                          |
| 26 | CSNA                  | Inverting input to aux current sense amplifier                                                                                                              |
| 27 | VBOOTA                | VBOOTA Voltage input pin. Set to adjust the aux boot-up voltage                                                                                             |
| 28 | PWMA/IMAXA            | Aux PWM output to gate driver. Also as ICC_MAXA input pin for aux rail. During start up it is used to program ICC_MAXA with a resistor to ground            |
| 29 | IMAX                  | ICC_MAX Input Pin for core rail. During start up it is used to program ICC_MAX with a resistor to ground                                                    |
| 30 | PWM2<br>(Rev 0)       | Phase 2 PWM output. Pull to Vcc will configure as 2-phase operation.                                                                                        |
|    | PWM2/ISHED<br>(Rev 1) | Phase 2 PWM output. Also as Phase shedding Input. During start up a resistor to ground on this pin programs the ISHED voltage.                              |
| 31 | PWM3/VBOOT            | Phase 3 PWM output. Also as VBOOT input pin to adjust the core rail boot-up voltage. During start up it is used to program VBOOT with a resistor to ground. |
| 32 | PWM1/ADDR             | Phase 1 PWM output. Also as Address program pin. A resistor to ground on this pin programs the SVID address of the device.                                  |
| 33 | DRON                  | Bidirectional gate drive enable for core output.                                                                                                            |
| 34 | CSP1                  | Non-inverting input to current balance sense amplifier for phase 1                                                                                          |
| 35 | CSN1                  | Inverting input to current balance sense amplifier for phase 1                                                                                              |
| 36 | CSP3                  | Non-inverting input to current balance sense amplifier for phase 3                                                                                          |
| 37 | CSN3                  | Inverting input to current balance sense amplifier for phase 3                                                                                              |
| 38 | CSP2                  | Non-inverting input to current balance sense amplifier for phase 2                                                                                          |
| 39 | CSN2                  | Inverting input to current balance sense amplifier for phase 2                                                                                              |
| 40 | NC                    | No connection                                                                                                                                               |
| 41 | NC                    | No connection                                                                                                                                               |
| 42 | CSREF                 | Total output current sense amplifier reference voltage input.                                                                                               |
| 43 | IOUT                  | Total output current monitor for core output.                                                                                                               |
| 44 | CSSUM                 | Inverting input of total current sense amplifier for core output.                                                                                           |
| 45 | CSCOMP                | Output of total current sense amplifier for core output.                                                                                                    |
| 46 | DROOP                 | Used to program droop function for core output. It's connected to the resistor divider placed between CSCOMP and CSREF summing node.                        |
| 47 | ILIM                  | Over current shutdown threshold setting for core output. Resistor to CSCOMP to set threshold.                                                               |
| 48 | COMP                  | Output of the error amplifier and the inverting inputs of the PWM comparators for the core output.                                                          |
| 49 | FB                    | Error amplifier voltage feedback for core output                                                                                                            |
| 50 | TRBST                 | Compensation pin for core rail load transient boost.                                                                                                        |
| 51 | VSN                   | Inverting input to the core differential remote sense amplifier.                                                                                            |

|    |            |                                                         |
|----|------------|---------------------------------------------------------|
| 52 | DIFFOUT    | Output of the core differential remote sense amplifier. |
| 53 | FLAG / GND | Power supply return ( QFN Flag )                        |

**Four Phase Plus One Phase Application Control Circuit**

**TBD**

## ABSOLUTE MAXIMUM RATINGS

### Electrical Information

| Pin Symbol           | V <sub>MAX</sub> | V <sub>MIN</sub> | I <sub>SOURCE</sub> | I <sub>SINK</sub> |
|----------------------|------------------|------------------|---------------------|-------------------|
| COMP, COMPA          | VCC+0.3V         | -0.3V            | 2mA                 | 2mA               |
| CSCOMP, CSCOMPA      | VCC+0.3V         | -0.3V            | 2mA                 | 2mA               |
| VSN                  | GND+300mV        | GND-300mV        | 1mA                 | 1mA               |
| DIFFOUT, DIFFOUTA    | VCC+0.3V         | -0.3V            | 2mA                 | 2mA               |
| VR_RDY, VR_RDYA      | VCC+0.3V         | -0.3V            | N/A                 | 2mA               |
| VCC                  | 6.5V             | -0.3V            | N/A                 | N/A               |
| ROSC                 | VCC+0.3V         | -0.3V            | 1mA                 | N/A               |
| IOOUT, IOOUTA Output | 1.1V             | -0.3V            |                     |                   |
| VRMP                 | +25V             | -0.3V            |                     |                   |
| All Other Pins       | VCC+0.3V         | -0.3V            |                     |                   |

\*All signals referenced to GND unless noted otherwise.

### Thermal Information

| Thermal Characteristic<br>QFN Package <sup>2)</sup> | R <sub>JA</sub>  | TBD         | °C/W |
|-----------------------------------------------------|------------------|-------------|------|
| Operating Junction Temperature Range <sup>3)</sup>  | T <sub>J</sub>   | -10 to 125  | °C   |
| Operating Ambient Temperature Range                 |                  | -10 to 100  | °C   |
| Maximum Storage Temperature Range                   | T <sub>STG</sub> | -40 to +150 | °C   |
| Moisture Sensitivity Level<br>QFN Package           | MSL              | 1           |      |

\*The maximum package power dissipation must be observed.

2) JESD 51-5 (1S2P Direct-Attach Method) with 0 LFM

3) JESD 51-7 (1S2P Direct-Attach Method) with 0 LFM

# NCP6151S (4+1)/NCP6131 (3+1) ELECTRICAL CHARACTERISTICS

Unless otherwise stated:  $-10^{\circ}\text{C} < T_A < 100^{\circ}\text{C}$ ;  $4.75\text{V} < V_{CC} < 5.25\text{V}$ ;  $C_{VCC} = 0.1\mu\text{F}$

| PARAMETER                             | TEST CONDITIONS                                                                                                                                          | MIN   | TYP | MAX   | UNITS |
|---------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-----|-------|-------|
| <b>ERROR AMPLIFIER</b>                |                                                                                                                                                          |       |     |       |       |
| Input Bias Current                    |                                                                                                                                                          | -400  |     | 400   | nA    |
| Open Loop DC Gain                     | CL = 20pF to GND,<br>RL = 10KΩ to GND                                                                                                                    |       | 80  |       | dB    |
| Open Loop Unity Gain Bandwidth        | CL = 20pF to GND,<br>RL = 10KΩ to GND                                                                                                                    |       | 60  |       | MHz   |
| Slew Rate                             | $\Delta V_{in} = 100\text{mV}$ , $G = -10\text{V/V}$ ,<br>$\Delta V_{out} = 1.5\text{V} \sim 2.5\text{V}$ ,<br>CL = 20pF to GND,<br>DC Load = 10k to GND |       | 20  |       | V/μs  |
| Maximum Output Voltage                | $I_{SOURCE} = 2.0\text{mA}$                                                                                                                              | 3.5   | -   | -     | V     |
| Minimum Output Voltage                | $I_{SINK} = 2.0\text{mA}$                                                                                                                                | -     | -   | 1     | V     |
| <b>Differential Summing Amplifier</b> |                                                                                                                                                          |       |     |       |       |
| Input Bias Current                    |                                                                                                                                                          | -400  | -   | 400   | nA    |
| VSP Input Voltage Range               |                                                                                                                                                          | -0.3  | -   | 3.0   | V     |
| VSN Input Voltage Range               |                                                                                                                                                          | -0.3  | -   | 0.3   | V     |
| -3dB Bandwidth                        | CL = 20pF to GND,<br>RL = 10KΩ to GND                                                                                                                    |       | 12  |       | MHz   |
| Closed Loop DC gain VS to Diffout     | $V_{S+}$ to $V_{S-} = 0.5$ to $1.3\text{V}$                                                                                                              |       | 1.0 |       | V/V   |
| Droop Accuracy                        | CSREF-DROOP=80mV<br>DAC=0.8V to 1.2V                                                                                                                     | -81.5 |     | -78.5 | mV    |
| Maximum Output Voltage                | $I_{SOURCE} = 2\text{mA}$                                                                                                                                | 3.0   | -   | -     | V     |
| Minimum Output Voltage                | $I_{SINK} = 2\text{mA}$                                                                                                                                  | -     | -   | 0.5   | V     |

**ELECTRICAL CHARACTERISTICS:**Unless otherwise stated:  $-10^{\circ}\text{C} < T_A < 100^{\circ}\text{C}$ ;  $4.75\text{V} < V_{CC} < 5.25\text{V}$ ;  $C_{VCC} = 0.1\mu\text{F}$ 

| PARAMETER                                 | TEST CONDITION                                                                         | MIN  | TYP | MAX | UNITS         |
|-------------------------------------------|----------------------------------------------------------------------------------------|------|-----|-----|---------------|
| <b>CURRENT SUMMING AMPLIFIER</b>          |                                                                                        |      |     |     |               |
| Offset Voltage ( $V_{os}$ )               |                                                                                        | -300 |     | 300 | $\mu\text{V}$ |
| Input Bias Current                        | $CSSUM = CSREF = 1\text{V}$                                                            | -7.5 |     | 7.5 | nA            |
| Open Loop Gain                            |                                                                                        |      | 80  |     | dB            |
| Current Sense Unity Gain Bandwidth        | $C_L = 20\text{pF}$ to GND,<br>$R_L = 10\text{K}\Omega$ to GND                         |      | 9   |     | MHz           |
| Maximum CSCOMP (A) Output Voltage         | $I_{source} = 2\text{mA}$                                                              | 3.5  | -   | -   | V             |
| Minimum CSCOMP(A) Output Voltage          | $I_{sink} = 500\mu\text{A}$                                                            | -    | -   | 0.1 | V             |
| <b>CURRENT BALANCE AMPLIFIER</b>          |                                                                                        |      |     |     |               |
| Input Bias Current                        | $CSPx = CSNx = 1.2\text{V}$                                                            | -50  | -   | 50  | nA            |
| Common Mode Input Voltage Range           | $CSPx = CSNx$                                                                          | 0    | -   | 2.0 | V             |
| Differential Mode Input Voltage Range     | $CSNx = 1.2\text{V}$                                                                   | -100 | -   | 100 | mV            |
| Closed loop Input Offset Voltage Matching | $CSPx = CSNx = 1.2\text{V}$ ,<br>Measured from the average                             | -1.5 | -   | 1.5 | mV            |
| Current Sense Amplifier Gain              | $0\text{V} < CSPx - CSNx < 0.1\text{V}$ ,                                              | 5.7  | 6.0 | 6.3 | V/V           |
| Multiphase Current Sense Gain Matching    | $CSN = CSP = 10\text{mV}$ to $30\text{mV}$                                             | -3   |     | 3   | %             |
| -3dB Bandwidth                            |                                                                                        |      | 8   |     | MHz           |
| <b>INPUT SUPPLY</b>                       |                                                                                        |      |     |     |               |
| $V_{CC}$ Quiescent Current                | $EN = \text{high}$                                                                     | TBD  | 30  | TBD | mA            |
|                                           | $EN = \text{low}$                                                                      | 35   | TBD | 70  | $\mu\text{A}$ |
| UVLO Threshold                            | $V_{CC}$ rising                                                                        |      |     | 4.5 | V             |
|                                           | $V_{CC}$ falling                                                                       | 4.1  |     |     | V             |
| $V_{CC}$ UVLO Hysteresis                  |                                                                                        |      | 200 |     | mV            |
| <b>DAC SLEW RATE</b>                      |                                                                                        |      |     |     |               |
| Soft Start Slew Rate                      |                                                                                        |      | TBD |     | mv/us         |
| Slew Rate Slow                            |                                                                                        |      | 5   |     | mv/us         |
| Slew Rate Fast                            |                                                                                        |      | 20  |     | mv/us         |
| AUX Soft Start Slew Rate                  |                                                                                        |      | TBD |     | mv/us         |
| AUX Slew Rate Slow                        |                                                                                        |      | 2.5 |     | mv/us         |
| AUX Slew Rate Fast                        |                                                                                        |      | 10  |     | mv/us         |
| <b>ENABLE INPUT</b>                       |                                                                                        |      |     |     |               |
| Enable High Input Leakage Current         | External 1K pull-up to 3.3V                                                            | -    |     | 1.0 | $\mu\text{A}$ |
| Upper Threshold                           | $V_{UPPER}$                                                                            | 0.8  |     |     | V             |
| Lower Threshold                           | $V_{LOWER}$                                                                            |      |     | 0.4 | V             |
| Total Hysteresis                          | $V_{UPPER} - V_{LOWER}$                                                                |      | 20  |     | mV            |
| Enable Delay Time                         | Measure time from Enable transitioning HI to when DRON goes high, $V_{boot}$ is not 0V |      |     | 5.0 | ms            |

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| PARAMETER                                                                 | TEST CONDITION                                                                                                                            | MIN   | TYP  | MAX   | UNITS         |
|---------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|-------|------|-------|---------------|
| <b>DRVON</b>                                                              |                                                                                                                                           |       |      |       |               |
| Output High Voltage                                                       | Sourcing 500uA                                                                                                                            | 3.5   |      |       | V             |
| Output Low Voltage                                                        | Sinking 500uA                                                                                                                             |       |      | 0.1   | V             |
| Rise/Fall Time                                                            | CL (PCB) = 20pF,<br>$\Delta V_o = 10\%$ to 90%                                                                                            | -     | 10   |       | ns            |
| Internal Pull Down Resistance                                             | EN = Low                                                                                                                                  |       | 70   |       | k $\Omega$    |
| <b>IOUT / IOUTA OUTPUT</b>                                                |                                                                                                                                           |       |      |       |               |
| Maximum Output Voltage                                                    | Rlim=5k                                                                                                                                   | 2.5   |      |       | V             |
| Input Referred Offset Voltage                                             | Ilimit to CSREF                                                                                                                           | -1    |      | 1     | mV            |
| Output Source Current                                                     | Ilimit sink current= 80uA                                                                                                                 |       |      | 800   | uA            |
| Current Gain                                                              | $(I_{OUT\_CURRENT}) / (I_{LIMIT\_CURRENT})$ , Rlim =<br>Riout = 8.0k $\Omega$ , Temp range: 0 $^{\circ}\text{C}$ to 60 $^{\circ}\text{C}$ | 9.5   | 10   | 10.5  |               |
| <b>OSCILLATOR</b>                                                         |                                                                                                                                           |       |      |       |               |
| Switching Frequency Range                                                 |                                                                                                                                           | 100   |      | 1500  | KHz           |
| Switching Frequency Accuracy                                              | 250KHz < Fsw < 1MHz                                                                                                                       | -10   |      | 10    | %             |
| 3 Phase Operation                                                         | Rt=6.98 k $\Omega$                                                                                                                        | 360   | 400  | 440   | kHz           |
| Rosc Output Voltage                                                       | Rt=6.98 k $\Omega$                                                                                                                        | 1.95  | 2.00 | 2.05  | V             |
| <b>OUTPUT OVER VOLTAGE &amp; UNDER VOLTAGE PROTECTION (OVP &amp; UVP)</b> |                                                                                                                                           |       |      |       |               |
| Over Voltage Threshold During Soft-Start                                  |                                                                                                                                           | 2.175 | 2.2  | 2.225 | V             |
| Over Voltage Threshold Above DAC                                          | VSP(A) rising                                                                                                                             | 150   | 175  | 200   | mV            |
| Over Voltage Delay                                                        | VSP(A) rising to PWMx low                                                                                                                 |       | 50   |       | ns            |
| Overvoltage Hysteresis                                                    | VSP(A) falling                                                                                                                            |       | 25   |       | mV            |
| Under Voltage Threshold Below DAC-DROOP                                   | VSP(A) falling                                                                                                                            | 250   | 300  | 350   | mV            |
| Under-voltage Hysteresis                                                  | VSP(A) rising                                                                                                                             |       | 25   |       | mV            |
| Under-voltage Delay                                                       |                                                                                                                                           |       | 5    |       | us            |
| <b>VR12 DAC</b>                                                           |                                                                                                                                           |       |      |       |               |
| System Voltage Accuracy                                                   | $1.0\text{V} \leq \text{DAC} < 1.52\text{V}$                                                                                              | -0.5  |      | 0.5   | %             |
|                                                                           | $0.8\text{V} < \text{DAC} < 0.995\text{V}$                                                                                                | -5    |      | 5     | mV            |
|                                                                           | $0.5\text{V} < \text{DAC} < 0.795\text{V}$                                                                                                | -8    |      | 8     | mV            |
|                                                                           | $0.25\text{V} < \text{DAC} < 0.495\text{V}$                                                                                               | -35   |      | 35    | mV            |
| Droop Feed-Forward Current                                                | Measure on DROOP pin                                                                                                                      | 60    | 66   | 72    | $\mu\text{A}$ |
| Droop Feed-Forward Pulse On-Time                                          |                                                                                                                                           |       | 0.16 |       | $\mu\text{s}$ |
| <b>OVERCURRENT PROTECTION</b>                                             |                                                                                                                                           |       |      |       |               |
| ILIM Threshold Current (OCP shutdown after 50 us delay)                   | (PS0) Rlim=20k                                                                                                                            | 9.0   | 10   | 11.0  | $\mu\text{A}$ |
| ILIM Threshold Current (immediate OCP shutdown)                           | SetPS = 00 (PS0)                                                                                                                          | 13.5  | 15   | 16.5  | $\mu\text{A}$ |
| Over-Current (DCR) Threshold                                              | During startup, CSP-CSN                                                                                                                   | 36    | 48   | 60    | mV            |
| Maximum Timer for OCP shutdown                                            |                                                                                                                                           |       | 55   |       | $\mu\text{s}$ |
| CSCOMP OCP Threshold                                                      |                                                                                                                                           |       | 50   |       | mV            |

**ELECTRICAL CHARACTERISTICS:**Unless otherwise stated:  $-10^{\circ}\text{C} < T_A < 100^{\circ}\text{C}$ ;  $4.75\text{V} < V_{CC} < 5.25\text{V}$ ;  $C_{VCC} = 0.1\mu\text{F}$ 

| PARAMETER                                              | TEST CONDITION                                                                                | MIN                    | TYP  | MAX   | UNITS         |
|--------------------------------------------------------|-----------------------------------------------------------------------------------------------|------------------------|------|-------|---------------|
| <b>MODULATORS (PWM COMPARATORS) FOR CORE &amp; AUX</b> |                                                                                               |                        |      |       |               |
| Minimum Pulse Width                                    | $F_{sw} = 350\text{KHz}$                                                                      |                        | 60   |       | ns            |
| 0% Duty Cycle                                          | COMP voltage when the PWM outputs remain LO                                                   |                        | 1.3  | -     | V             |
| 100% Duty Cycle                                        | COMP voltage when the PWM outputs remain HI - $VRMP = 12.0\text{V}$                           | -                      | 2.5  | -     | V             |
| PWM Ramp Duty Cycle Matching                           | COMP=2V, PWM Ton matching                                                                     |                        | TBD  |       | %             |
| PWM Phase Angle Error                                  | Between adjacent phases                                                                       | -10                    |      | 10    | deg           |
| Ramp Feed-forward Voltage range                        |                                                                                               | 5                      |      | 20    | V             |
| <b>TRBST</b>                                           |                                                                                               |                        |      |       |               |
| Output Low Voltage                                     | $I_{Sink} = 500\mu\text{A}$                                                                   |                        |      | TBD   | mV            |
| <b>TRBSTA</b>                                          |                                                                                               |                        |      |       |               |
| Output Low Voltage                                     | $I_{Sink} = 500\mu\text{A}$                                                                   |                        |      | TBD   | mV            |
| <b>VR_HOT#</b>                                         |                                                                                               |                        |      |       |               |
| Output Low Voltage                                     | $I_{VRHOT} = -4\text{mA}$                                                                     |                        |      | 0.3   | V             |
| Output Leakage Current                                 | High Impedance State                                                                          | -1.0                   | -    | 1.0   | $\mu\text{A}$ |
| <b>TSENSE/TSENSEA</b>                                  |                                                                                               |                        |      |       |               |
| Alert# Assert Threshold                                | NTC=100k in parallel with 8.2k @97C                                                           |                        | 483  |       | mV            |
| Alert# De-assert Threshold                             | NTC=100k in parallel with 8.2k @94C                                                           |                        | 503  |       | mV            |
| VRHOT Assert Threshold                                 | NTC=100k in parallel with 8.2k @100C                                                          |                        | 462  |       | mV            |
| VRHOT Rising Threshold                                 | NTC=100k in parallel with 8.2k @97C                                                           |                        | 483  |       | mV            |
| TSENSE Bias Current                                    |                                                                                               | 117.6                  | -120 | 122.4 | $\mu\text{A}$ |
| <b>ADC</b>                                             |                                                                                               |                        |      |       |               |
| Voltage Range                                          |                                                                                               | 0                      |      | 2     | V             |
| Total Unadjusted Error (TUE)                           |                                                                                               | -1                     |      | +1    | %             |
| Differential Nonlinearity (DNL)                        | 8-bit                                                                                         |                        |      | 1     | LSB           |
| Power Supply Sensitivity                               |                                                                                               |                        | +/-1 |       | %             |
| Conversion Time                                        |                                                                                               |                        | 30   |       | $\mu\text{s}$ |
| Round Robin                                            |                                                                                               |                        | 90   |       | $\mu\text{s}$ |
| <b>VR_RDY, VR_RDYA (POWER GOOD) OUTPUT</b>             |                                                                                               |                        |      |       |               |
| Output Low Saturation Voltage                          | $I_{VR\_RDY(A)} = 4\text{mA}$                                                                 | -                      | -    | 0.3   | V             |
| Rise Time                                              | External pull-up of 1K $\Omega$ to 3.3V, $C_{TOT} = 45\text{pF}$ , $\Delta V_o = 10\%$ to 90% | -                      | 100  |       | ns            |
| Fall Time                                              | External pull-up of 1K $\Omega$ to 3.3V, $C_{TOT} = 45\text{pF}$ , $\Delta V_o = 90\%$ to 10% | -                      | 10   |       | ns            |
| Output Voltage at Power-up                             | VR_RDY, VR_RDYA pulled up to 5V via 2K $\Omega$                                               | -                      | -    | 1.0   | V             |
| Output Leakage Current When High                       | VR_RDY & VR_RDYA = 5.0V                                                                       | -1.0                   | -    | 1.0   | $\mu\text{A}$ |
| VR_RDY Delay (rising)                                  | DAC=TARGET to VR_RDY                                                                          |                        | 500  |       | $\mu\text{s}$ |
| VR_RDY Delay (falling)                                 | From OCP or OVP                                                                               | -                      | 5    | -     | $\mu\text{s}$ |
| <b>PWM Outputs</b>                                     |                                                                                               |                        |      |       |               |
| Output High Voltage                                    | Sourcing 500 $\mu\text{A}$                                                                    | $V_{CC} - 0.1\text{V}$ | -    | -     | V             |
| Output Mid Voltage                                     | No Load, SetPS=02                                                                             | 1.9                    | 2.0  | 2.1   | V             |
| Output Low Voltage                                     | Sinking 500 $\mu\text{A}$                                                                     | -                      | -    | 0.7   | V             |
| Rise and Fall Time                                     | CL (PCB) = 50pF, $\Delta V_o = \text{GND to } V_{CC}$                                         | -                      | 10   |       | ns            |
| <b>2/3/4 Phase Detection</b>                           |                                                                                               |                        |      |       |               |
| PWM Pin Source Current                                 |                                                                                               |                        | 100  |       | $\mu\text{A}$ |
| PWM Pin Threshold Voltage                              |                                                                                               |                        | 2.5  |       | V             |
| Phase Detect Timer                                     |                                                                                               |                        | 50   |       | $\mu\text{s}$ |
| <b>SCLK, SDIO</b>                                      |                                                                                               |                        |      |       |               |
| VIL                                                    | Input Low Voltage                                                                             | 0.45                   |      |       | V             |
| VIH                                                    | Input High Voltage                                                                            |                        |      | 0.65  | V             |
| VHYS                                                   | Hysteresis Voltage                                                                            | 50                     |      |       | mV            |
| VOH                                                    | Output High Voltage                                                                           |                        | 1.05 |       | V             |
| VOL                                                    | Output Low Voltage (SDIO only)                                                                |                        | TBD  |       | mV            |

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| Parameter                                 | Test Condition                                      | MIN  | TYP | MAX | Units         |
|-------------------------------------------|-----------------------------------------------------|------|-----|-----|---------------|
| R <sub>ON</sub>                           | Buffer On Resistance (data line, ALERT#, and VRHOT) | 4    |     | 13  | $\Omega$      |
| Leakage Current                           |                                                     | -100 |     | 100 | $\mu\text{A}$ |
| Pad Capacitance                           |                                                     |      |     | 4.0 | pF            |
| VR clock to data delay (T <sub>co</sub> ) |                                                     | 4    |     | 8.3 | ns            |
| Setup time (T <sub>su</sub> )             |                                                     | 7    |     |     | ns            |
| Hold time (T <sub>hd</sub> )              |                                                     | 14   |     |     | ns            |
|                                           |                                                     |      |     |     |               |

**Table 2: VR12 VID Codes**

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Voltage (V) | HEX |
|------|------|------|------|------|------|------|------|-------------|-----|
| 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | OFF         | 00  |
| 0    | 0    | 0    | 0    | 0    | 0    | 0    | 1    | 0.25000     | 01  |
| 0    | 0    | 0    | 0    | 0    | 0    | 1    | 0    | 0.25500     | 02  |
| 0    | 0    | 0    | 0    | 0    | 0    | 1    | 1    | 0.26000     | 03  |
| 0    | 0    | 0    | 0    | 0    | 1    | 0    | 0    | 0.26500     | 04  |
| 0    | 0    | 0    | 0    | 0    | 1    | 0    | 1    | 0.27000     | 05  |
| 0    | 0    | 0    | 0    | 0    | 1    | 1    | 0    | 0.27500     | 06  |
| 0    | 0    | 0    | 0    | 0    | 1    | 1    | 1    | 0.28000     | 07  |
| 0    | 0    | 0    | 0    | 1    | 0    | 0    | 0    | 0.28500     | 08  |
| 0    | 0    | 0    | 0    | 1    | 0    | 0    | 1    | 0.29000     | 09  |
| 0    | 0    | 0    | 0    | 1    | 0    | 1    | 0    | 0.29500     | 0A  |
| 0    | 0    | 0    | 0    | 1    | 0    | 1    | 1    | 0.30000     | 0B  |
| 0    | 0    | 0    | 0    | 1    | 1    | 0    | 0    | 0.30500     | 0C  |
| 0    | 0    | 0    | 0    | 1    | 1    | 0    | 1    | 0.31000     | 0D  |
| 0    | 0    | 0    | 0    | 1    | 1    | 1    | 0    | 0.31500     | 0E  |
| 0    | 0    | 0    | 0    | 1    | 1    | 1    | 1    | 0.32000     | 0F  |
| 0    | 0    | 0    | 1    | 0    | 0    | 0    | 0    | 0.32500     | 10  |
| 0    | 0    | 0    | 1    | 0    | 0    | 0    | 1    | 0.33000     | 11  |
| 0    | 0    | 0    | 1    | 0    | 0    | 1    | 0    | 0.33500     | 12  |
| 0    | 0    | 0    | 1    | 0    | 0    | 1    | 1    | 0.34000     | 13  |
| 0    | 0    | 0    | 1    | 0    | 1    | 0    | 0    | 0.34500     | 14  |
| 0    | 0    | 0    | 1    | 0    | 1    | 0    | 1    | 0.35000     | 15  |
| 0    | 0    | 0    | 1    | 0    | 1    | 1    | 0    | 0.35500     | 16  |
| 0    | 0    | 0    | 1    | 0    | 1    | 1    | 1    | 0.36000     | 17  |
| 0    | 0    | 0    | 1    | 1    | 0    | 0    | 0    | 0.36500     | 18  |
| 0    | 0    | 0    | 1    | 1    | 0    | 0    | 1    | 0.37000     | 19  |
| 0    | 0    | 0    | 1    | 1    | 0    | 1    | 0    | 0.37500     | 1A  |
| 0    | 0    | 0    | 1    | 1    | 0    | 1    | 1    | 0.38000     | 1B  |
| 0    | 0    | 0    | 1    | 1    | 1    | 0    | 0    | 0.38500     | 1C  |
| 0    | 0    | 0    | 1    | 1    | 1    | 0    | 1    | 0.39000     | 1D  |
| 0    | 0    | 0    | 1    | 1    | 1    | 1    | 0    | 0.39500     | 1E  |
| 0    | 0    | 0    | 1    | 1    | 1    | 1    | 1    | 0.40000     | 1F  |
| 0    | 0    | 1    | 0    | 0    | 0    | 0    | 0    | 0.40500     | 20  |
| 0    | 0    | 1    | 0    | 0    | 0    | 0    | 1    | 0.41000     | 21  |
| 0    | 0    | 1    | 0    | 0    | 0    | 1    | 0    | 0.41500     | 22  |
| 0    | 0    | 1    | 0    | 0    | 0    | 1    | 1    | 0.42000     | 23  |
| 0    | 0    | 1    | 0    | 0    | 1    | 0    | 0    | 0.42500     | 24  |
| 0    | 0    | 1    | 0    | 0    | 1    | 0    | 1    | 0.43000     | 25  |
| 0    | 0    | 1    | 0    | 0    | 1    | 1    | 0    | 0.43500     | 26  |

Table 2: VR12 VID Codes (cont'd)

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Voltage (V) | HEX |
|------|------|------|------|------|------|------|------|-------------|-----|
| 0    | 0    | 1    | 0    | 0    | 1    | 1    | 1    | 0.44000     | 27  |
| 0    | 0    | 1    | 0    | 1    | 0    | 0    | 0    | 0.44500     | 28  |
| 0    | 0    | 1    | 0    | 1    | 0    | 0    | 1    | 0.45000     | 29  |
| 0    | 0    | 1    | 0    | 1    | 0    | 1    | 0    | 0.45500     | 2A  |
| 0    | 0    | 1    | 0    | 1    | 0    | 1    | 1    | 0.46000     | 2B  |
| 0    | 0    | 1    | 0    | 1    | 1    | 0    | 0    | 0.46500     | 2C  |
| 0    | 0    | 1    | 0    | 1    | 1    | 0    | 1    | 0.47000     | 2D  |
| 0    | 0    | 1    | 0    | 1    | 1    | 1    | 0    | 0.47500     | 2E  |
| 0    | 0    | 1    | 0    | 1    | 1    | 1    | 1    | 0.48000     | 2F  |
| 0    | 0    | 1    | 1    | 0    | 0    | 0    | 0    | 0.48500     | 30  |
| 0    | 0    | 1    | 1    | 0    | 0    | 0    | 1    | 0.49000     | 31  |
| 0    | 0    | 1    | 1    | 0    | 0    | 1    | 0    | 0.49500     | 32  |
| 0    | 0    | 1    | 1    | 0    | 0    | 1    | 1    | 0.50000     | 33  |
| 0    | 0    | 1    | 1    | 0    | 1    | 0    | 0    | 0.50500     | 34  |
| 0    | 0    | 1    | 1    | 0    | 1    | 0    | 1    | 0.51000     | 35  |
| 0    | 0    | 1    | 1    | 0    | 1    | 1    | 0    | 0.51500     | 36  |
| 0    | 0    | 1    | 1    | 0    | 1    | 1    | 1    | 0.52000     | 37  |
| 0    | 0    | 1    | 1    | 1    | 0    | 0    | 0    | 0.52500     | 38  |
| 0    | 0    | 1    | 1    | 1    | 0    | 0    | 1    | 0.53000     | 39  |
| 0    | 0    | 1    | 1    | 1    | 0    | 1    | 0    | 0.53500     | 3A  |
| 0    | 0    | 1    | 1    | 1    | 0    | 1    | 1    | 0.54000     | 3B  |
| 0    | 0    | 1    | 1    | 1    | 1    | 0    | 0    | 0.54500     | 3C  |
| 0    | 0    | 1    | 1    | 1    | 1    | 0    | 1    | 0.55000     | 3D  |
| 0    | 0    | 1    | 1    | 1    | 1    | 1    | 0    | 0.55500     | 3E  |
| 0    | 0    | 1    | 1    | 1    | 1    | 1    | 1    | 0.56000     | 3F  |
| 0    | 1    | 0    | 0    | 0    | 0    | 0    | 0    | 0.56500     | 40  |
| 0    | 1    | 0    | 0    | 0    | 0    | 0    | 1    | 0.57000     | 41  |
| 0    | 1    | 0    | 0    | 0    | 0    | 1    | 0    | 0.57500     | 42  |
| 0    | 1    | 0    | 0    | 0    | 0    | 1    | 1    | 0.58000     | 43  |
| 0    | 1    | 0    | 0    | 0    | 1    | 0    | 0    | 0.58500     | 44  |
| 0    | 1    | 0    | 0    | 0    | 1    | 0    | 1    | 0.59000     | 45  |
| 0    | 1    | 0    | 0    | 0    | 1    | 1    | 0    | 0.59500     | 46  |
| 0    | 1    | 0    | 0    | 0    | 1    | 1    | 1    | 0.60000     | 47  |
| 0    | 1    | 0    | 0    | 1    | 0    | 0    | 0    | 0.60500     | 48  |
| 0    | 1    | 0    | 0    | 1    | 0    | 0    | 1    | 0.61000     | 49  |
| 0    | 1    | 0    | 0    | 1    | 0    | 1    | 0    | 0.61500     | 4A  |
| 0    | 1    | 0    | 0    | 1    | 0    | 1    | 1    | 0.62000     | 4B  |
| 0    | 1    | 0    | 0    | 1    | 1    | 0    | 0    | 0.62500     | 4C  |
| 0    | 1    | 0    | 0    | 1    | 1    | 0    | 1    | 0.63000     | 4D  |
| 0    | 1    | 0    | 0    | 1    | 1    | 1    | 0    | 0.63500     | 4E  |
| 0    | 1    | 0    | 0    | 1    | 1    | 1    | 1    | 0.64000     | 4F  |
| 0    | 1    | 0    | 1    | 0    | 0    | 0    | 0    | 0.64500     | 50  |
| 0    | 1    | 0    | 1    | 0    | 0    | 0    | 1    | 0.65000     | 51  |
| 0    | 1    | 0    | 1    | 0    | 0    | 1    | 0    | 0.65500     | 52  |
| 0    | 1    | 0    | 1    | 0    | 0    | 1    | 1    | 0.66000     | 53  |
| 0    | 1    | 0    | 1    | 0    | 1    | 0    | 0    | 0.66500     | 54  |
| 0    | 1    | 0    | 1    | 0    | 1    | 0    | 1    | 0.67000     | 55  |
| 0    | 1    | 0    | 1    | 0    | 1    | 1    | 0    | 0.67500     | 56  |
| 0    | 1    | 0    | 1    | 0    | 1    | 1    | 1    | 0.68000     | 57  |
| 0    | 1    | 0    | 1    | 1    | 0    | 0    | 0    | 0.68500     | 58  |

Table 2: VR12 VID Codes (cont'd)

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Voltage (V) | HEX |
|------|------|------|------|------|------|------|------|-------------|-----|
| 0    | 1    | 0    | 1    | 1    | 0    | 0    | 1    | 0.69000     | 59  |
| 0    | 1    | 0    | 1    | 1    | 0    | 1    | 0    | 0.69500     | 5A  |
| 0    | 1    | 0    | 1    | 1    | 0    | 1    | 1    | 0.70000     | 5B  |
| 0    | 1    | 0    | 1    | 1    | 1    | 0    | 0    | 0.70500     | 5C  |
| 0    | 1    | 0    | 1    | 1    | 1    | 0    | 1    | 0.71000     | 5D  |
| 0    | 1    | 0    | 1    | 1    | 1    | 1    | 0    | 0.71500     | 5E  |
| 0    | 1    | 0    | 1    | 1    | 1    | 1    | 1    | 0.72000     | 5F  |
| 0    | 1    | 1    | 0    | 0    | 0    | 0    | 0    | 0.72500     | 60  |
| 0    | 1    | 1    | 0    | 0    | 0    | 0    | 1    | 0.73000     | 61  |
| 0    | 1    | 1    | 0    | 0    | 0    | 1    | 0    | 0.73500     | 62  |
| 0    | 1    | 1    | 0    | 0    | 0    | 1    | 1    | 0.74000     | 63  |
| 0    | 1    | 1    | 0    | 0    | 1    | 0    | 0    | 0.74500     | 64  |
| 0    | 1    | 1    | 0    | 0    | 1    | 0    | 1    | 0.75000     | 65  |
| 0    | 1    | 1    | 0    | 0    | 1    | 1    | 0    | 0.75500     | 66  |
| 0    | 1    | 1    | 0    | 0    | 1    | 1    | 1    | 0.76000     | 67  |
| 0    | 1    | 1    | 0    | 1    | 0    | 0    | 0    | 0.76500     | 68  |
| 0    | 1    | 1    | 0    | 1    | 0    | 0    | 1    | 0.77000     | 69  |
| 0    | 1    | 1    | 0    | 1    | 0    | 1    | 0    | 0.77500     | 6A  |
| 0    | 1    | 1    | 0    | 1    | 0    | 1    | 1    | 0.78000     | 6B  |
| 0    | 1    | 1    | 0    | 1    | 1    | 0    | 0    | 0.78500     | 6C  |
| 0    | 1    | 1    | 0    | 1    | 1    | 0    | 1    | 0.79000     | 6D  |
| 0    | 1    | 1    | 0    | 1    | 1    | 1    | 0    | 0.79500     | 6E  |
| 0    | 1    | 1    | 0    | 1    | 1    | 1    | 1    | 0.80000     | 6F  |
| 0    | 1    | 1    | 1    | 0    | 0    | 0    | 0    | 0.80500     | 70  |
| 0    | 1    | 1    | 1    | 0    | 0    | 0    | 1    | 0.81000     | 71  |
| 0    | 1    | 1    | 1    | 0    | 0    | 1    | 0    | 0.81500     | 72  |
| 0    | 1    | 1    | 1    | 0    | 0    | 1    | 1    | 0.82000     | 73  |
| 0    | 1    | 1    | 1    | 0    | 1    | 0    | 0    | 0.82500     | 74  |
| 0    | 1    | 1    | 1    | 0    | 1    | 0    | 1    | 0.83000     | 75  |
| 0    | 1    | 1    | 1    | 0    | 1    | 1    | 0    | 0.83500     | 76  |
| 0    | 1    | 1    | 1    | 0    | 1    | 1    | 1    | 0.84000     | 77  |
| 0    | 1    | 1    | 1    | 1    | 0    | 0    | 0    | 0.84500     | 78  |
| 0    | 1    | 1    | 1    | 1    | 0    | 0    | 1    | 0.85000     | 79  |
| 0    | 1    | 1    | 1    | 1    | 0    | 1    | 0    | 0.85500     | 7A  |
| 0    | 1    | 1    | 1    | 1    | 0    | 1    | 1    | 0.86000     | 7B  |
| 0    | 1    | 1    | 1    | 1    | 1    | 0    | 0    | 0.86500     | 7C  |
| 0    | 1    | 1    | 1    | 1    | 1    | 0    | 1    | 0.87000     | 7D  |
| 0    | 1    | 1    | 1    | 1    | 1    | 1    | 0    | 0.87500     | 7E  |
| 0    | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 0.88000     | 7F  |
| 1    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0.88500     | 80  |
| 1    | 0    | 0    | 0    | 0    | 0    | 0    | 1    | 0.89000     | 81  |
| 1    | 0    | 0    | 0    | 0    | 0    | 1    | 0    | 0.89500     | 82  |
| 1    | 0    | 0    | 0    | 0    | 0    | 1    | 1    | 0.90000     | 83  |
| 1    | 0    | 0    | 0    | 0    | 1    | 0    | 0    | 0.90500     | 84  |
| 1    | 0    | 0    | 0    | 0    | 1    | 0    | 1    | 0.91000     | 85  |
| 1    | 0    | 0    | 0    | 0    | 1    | 1    | 0    | 0.91500     | 86  |
| 1    | 0    | 0    | 0    | 0    | 1    | 1    | 1    | 0.92000     | 87  |
| 1    | 0    | 0    | 0    | 1    | 0    | 0    | 0    | 0.92500     | 88  |
| 1    | 0    | 0    | 0    | 1    | 0    | 0    | 1    | 0.93000     | 89  |
| 1    | 0    | 0    | 0    | 1    | 0    | 1    | 0    | 0.93500     | 8A  |
| 1    | 0    | 0    | 0    | 1    | 0    | 1    | 1    | 0.94000     | 8B  |

Table 2: VR12 VID Codes (cont'd)

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Voltage (V) | HEX |
|------|------|------|------|------|------|------|------|-------------|-----|
| 1    | 0    | 0    | 0    | 1    | 1    | 0    | 0    | 0.94500     | 8C  |
| 1    | 0    | 0    | 0    | 1    | 1    | 0    | 1    | 0.95000     | 8D  |
| 1    | 0    | 0    | 0    | 1    | 1    | 1    | 0    | 0.95500     | 8E  |
| 1    | 0    | 0    | 0    | 1    | 1    | 1    | 1    | 0.96000     | 8F  |
| 1    | 0    | 0    | 1    | 0    | 0    | 0    | 0    | 0.96500     | 90  |
| 1    | 0    | 0    | 1    | 0    | 0    | 0    | 1    | 0.97000     | 91  |
| 1    | 0    | 0    | 1    | 0    | 0    | 1    | 0    | 0.97500     | 92  |
| 1    | 0    | 0    | 1    | 0    | 0    | 1    | 1    | 0.98000     | 93  |
| 1    | 0    | 0    | 1    | 0    | 1    | 0    | 0    | 0.98500     | 94  |
| 1    | 0    | 0    | 1    | 0    | 1    | 0    | 1    | 0.99000     | 95  |
| 1    | 0    | 0    | 1    | 0    | 1    | 1    | 0    | 0.99500     | 96  |
| 1    | 0    | 0    | 1    | 0    | 1    | 1    | 1    | 1.00000     | 97  |
| 1    | 0    | 0    | 1    | 1    | 0    | 0    | 0    | 1.00500     | 98  |
| 1    | 0    | 0    | 1    | 1    | 0    | 0    | 1    | 1.01000     | 99  |
| 1    | 0    | 0    | 1    | 1    | 0    | 1    | 0    | 1.01500     | 9A  |
| 1    | 0    | 0    | 1    | 1    | 0    | 1    | 1    | 1.02000     | 9B  |
| 1    | 0    | 0    | 1    | 1    | 1    | 0    | 0    | 1.02500     | 9C  |
| 1    | 0    | 0    | 1    | 1    | 1    | 0    | 1    | 1.03000     | 9D  |
| 1    | 0    | 0    | 1    | 1    | 1    | 1    | 0    | 1.03500     | 9E  |
| 1    | 0    | 0    | 1    | 1    | 1    | 1    | 1    | 1.04000     | 9F  |
| 1    | 0    | 1    | 0    | 0    | 0    | 0    | 0    | 1.04500     | A0  |
| 1    | 0    | 1    | 0    | 0    | 0    | 0    | 1    | 1.05000     | A1  |
| 1    | 0    | 1    | 0    | 0    | 0    | 1    | 0    | 1.05500     | A2  |
| 1    | 0    | 1    | 0    | 0    | 0    | 1    | 1    | 1.06000     | A3  |
| 1    | 0    | 1    | 0    | 0    | 1    | 0    | 0    | 1.06500     | A4  |
| 1    | 0    | 1    | 0    | 0    | 1    | 0    | 1    | 1.07000     | A5  |
| 1    | 0    | 1    | 0    | 0    | 1    | 1    | 0    | 1.07500     | A6  |
| 1    | 0    | 1    | 0    | 0    | 1    | 1    | 1    | 1.08000     | A7  |
| 1    | 0    | 1    | 0    | 1    | 0    | 0    | 0    | 1.08500     | A8  |
| 1    | 0    | 1    | 0    | 1    | 0    | 0    | 1    | 1.09000     | A9  |
| 1    | 0    | 1    | 0    | 1    | 0    | 1    | 0    | 1.09500     | AA  |
| 1    | 0    | 1    | 0    | 1    | 0    | 1    | 1    | 1.10000     | AB  |
| 1    | 0    | 1    | 0    | 1    | 1    | 0    | 0    | 1.10500     | AC  |
| 1    | 0    | 1    | 0    | 1    | 1    | 0    | 1    | 1.11000     | AD  |
| 1    | 0    | 1    | 0    | 1    | 1    | 1    | 0    | 1.11500     | AE  |
| 1    | 0    | 1    | 0    | 1    | 1    | 1    | 1    | 1.12000     | AF  |
| 1    | 0    | 1    | 1    | 0    | 0    | 0    | 0    | 1.12500     | B0  |
| 1    | 0    | 1    | 1    | 0    | 0    | 0    | 1    | 1.13000     | B1  |
| 1    | 0    | 1    | 1    | 0    | 0    | 1    | 0    | 1.13500     | B2  |
| 1    | 0    | 1    | 1    | 0    | 0    | 1    | 1    | 1.14000     | B3  |
| 1    | 0    | 1    | 1    | 0    | 1    | 0    | 0    | 1.14500     | B4  |

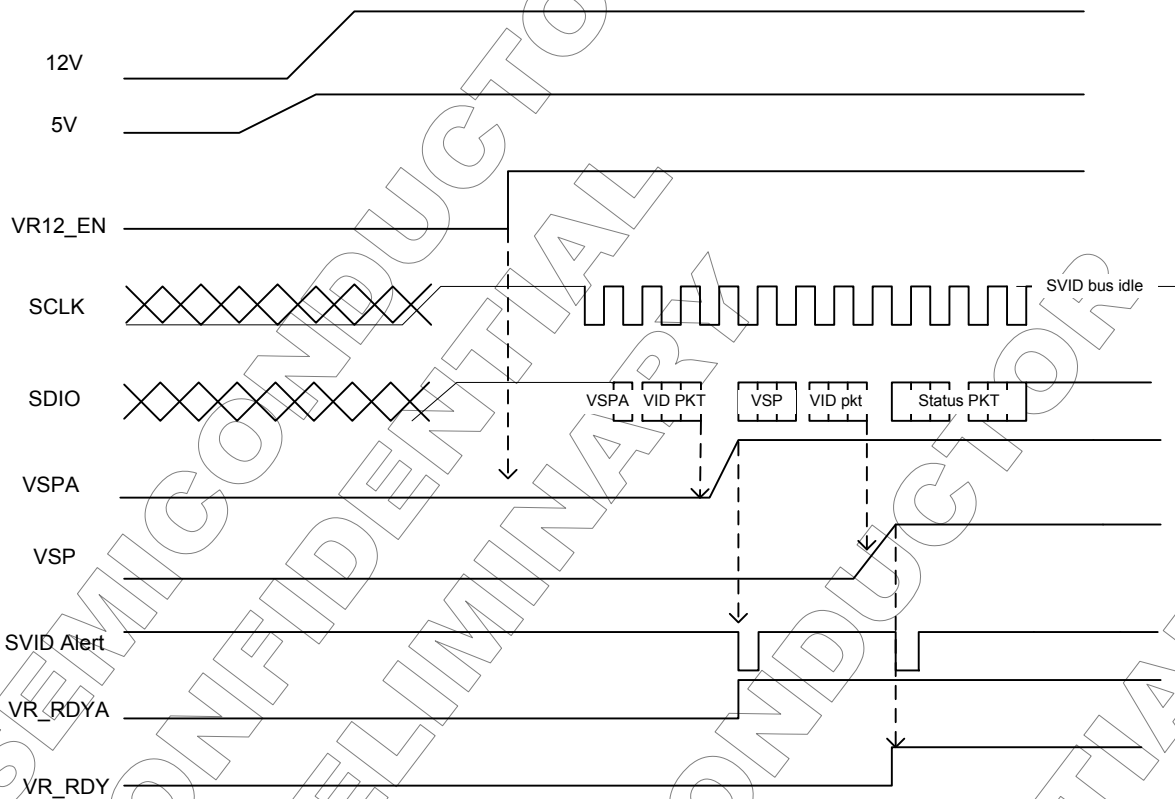
**Table 2: VR12 VID Codes (cont'd)**

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Voltage (V) | HEX |
|------|------|------|------|------|------|------|------|-------------|-----|
| 1    | 0    | 1    | 1    | 0    | 1    | 0    | 1    | 1.15000     | B5  |
| 1    | 0    | 1    | 1    | 0    | 1    | 1    | 0    | 1.15500     | B6  |
| 1    | 0    | 1    | 1    | 0    | 1    | 1    | 1    | 1.16000     | B7  |
| 1    | 0    | 1    | 1    | 1    | 0    | 0    | 0    | 1.16500     | B8  |
| 1    | 0    | 1    | 1    | 1    | 0    | 0    | 1    | 1.17000     | B9  |
| 1    | 0    | 1    | 1    | 1    | 0    | 1    | 0    | 1.17500     | BA  |
| 1    | 0    | 1    | 1    | 1    | 0    | 1    | 1    | 1.18000     | BB  |
| 1    | 0    | 1    | 1    | 1    | 1    | 0    | 0    | 1.18500     | BC  |
| 1    | 0    | 1    | 1    | 1    | 1    | 0    | 1    | 1.19000     | BD  |
| 1    | 0    | 1    | 1    | 1    | 1    | 1    | 0    | 1.19500     | BE  |
| 1    | 0    | 1    | 1    | 1    | 1    | 1    | 1    | 1.20000     | BF  |
| 1    | 1    | 0    | 0    | 0    | 0    | 0    | 0    | 1.20500     | C0  |
| 1    | 1    | 0    | 0    | 0    | 0    | 0    | 1    | 1.21000     | C1  |
| 1    | 1    | 0    | 0    | 0    | 0    | 1    | 0    | 1.21500     | C2  |
| 1    | 1    | 0    | 0    | 0    | 0    | 1    | 1    | 1.22000     | C3  |
| 1    | 1    | 0    | 0    | 0    | 1    | 0    | 0    | 1.22500     | C4  |
| 1    | 1    | 0    | 0    | 0    | 1    | 0    | 1    | 1.23000     | C5  |
| 1    | 1    | 0    | 0    | 0    | 1    | 1    | 0    | 1.23500     | C6  |
| 1    | 1    | 0    | 0    | 0    | 1    | 1    | 1    | 1.24000     | C7  |
| 1    | 1    | 0    | 0    | 1    | 0    | 0    | 0    | 1.24500     | C8  |
| 1    | 1    | 0    | 0    | 1    | 0    | 0    | 1    | 1.25000     | C9  |
| 1    | 1    | 0    | 0    | 1    | 0    | 1    | 0    | 1.25500     | CA  |
| 1    | 1    | 0    | 0    | 1    | 0    | 1    | 1    | 1.26000     | CB  |
| 1    | 1    | 0    | 0    | 1    | 1    | 0    | 0    | 1.26500     | CC  |
| 1    | 1    | 0    | 0    | 1    | 1    | 0    | 1    | 1.27000     | CD  |
| 1    | 1    | 0    | 0    | 1    | 1    | 1    | 0    | 1.27500     | CE  |
| 1    | 1    | 0    | 0    | 1    | 1    | 1    | 1    | 1.28000     | CF  |
| 1    | 1    | 0    | 1    | 0    | 0    | 0    | 0    | 1.28500     | D0  |
| 1    | 1    | 0    | 1    | 0    | 0    | 0    | 1    | 1.29000     | D1  |
| 1    | 1    | 0    | 1    | 0    | 0    | 1    | 0    | 1.29500     | D2  |
| 1    | 1    | 0    | 1    | 0    | 0    | 1    | 1    | 1.30000     | D3  |
| 1    | 1    | 0    | 1    | 0    | 1    | 0    | 0    | 1.30500     | D4  |
| 1    | 1    | 0    | 1    | 0    | 1    | 0    | 1    | 1.31000     | D5  |
| 1    | 1    | 0    | 1    | 0    | 1    | 1    | 0    | 1.31500     | D6  |
| 1    | 1    | 0    | 1    | 0    | 1    | 1    | 1    | 1.32000     | D7  |
| 1    | 1    | 0    | 1    | 1    | 0    | 0    | 0    | 1.32500     | D8  |
| 1    | 1    | 0    | 1    | 1    | 0    | 0    | 1    | 1.33000     | D9  |
| 1    | 1    | 0    | 1    | 1    | 0    | 1    | 0    | 1.33500     | DA  |
| 1    | 1    | 0    | 1    | 1    | 0    | 1    | 1    | 1.34000     | DB  |
| 1    | 1    | 0    | 1    | 1    | 1    | 0    | 0    | 1.34500     | DC  |
| 1    | 1    | 0    | 1    | 1    | 1    | 0    | 1    | 1.35000     | DD  |

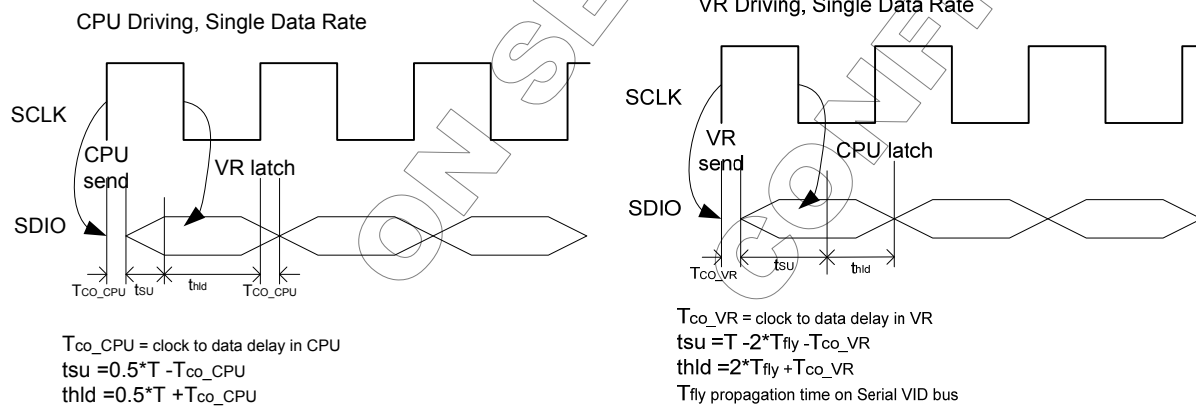
**Table 2: VR12 VID Codes (cont'd)**

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | Voltage (V) | HEX |
|------|------|------|------|------|------|------|------|-------------|-----|
| 1    | 1    | 0    | 1    | 1    | 1    | 1    | 0    | 1.35500     | DE  |
| 1    | 1    | 0    | 1    | 1    | 1    | 1    | 1    | 1.36000     | DF  |
| 1    | 1    | 1    | 0    | 0    | 0    | 0    | 0    | 1.36500     | E0  |
| 1    | 1    | 1    | 0    | 0    | 0    | 0    | 1    | 1.37000     | E1  |
| 1    | 1    | 1    | 0    | 0    | 0    | 1    | 0    | 1.37500     | E2  |
| 1    | 1    | 1    | 0    | 0    | 0    | 1    | 1    | 1.38000     | E3  |
| 1    | 1    | 1    | 0    | 0    | 1    | 0    | 0    | 1.38500     | E4  |
| 1    | 1    | 1    | 0    | 0    | 1    | 0    | 1    | 1.39000     | E5  |
| 1    | 1    | 1    | 0    | 0    | 1    | 1    | 0    | 1.39500     | E6  |
| 1    | 1    | 1    | 0    | 0    | 1    | 1    | 1    | 1.40000     | E7  |
| 1    | 1    | 1    | 0    | 1    | 0    | 0    | 0    | 1.40500     | E8  |
| 1    | 1    | 1    | 0    | 1    | 0    | 0    | 1    | 1.41000     | E9  |
| 1    | 1    | 1    | 0    | 1    | 0    | 1    | 0    | 1.41500     | EA  |
| 1    | 1    | 1    | 0    | 1    | 0    | 1    | 1    | 1.42000     | EB  |
| 1    | 1    | 1    | 0    | 1    | 1    | 0    | 0    | 1.42500     | EC  |
| 1    | 1    | 1    | 0    | 1    | 1    | 0    | 1    | 1.43000     | ED  |
| 1    | 1    | 1    | 0    | 1    | 1    | 1    | 0    | 1.43500     | EE  |
| 1    | 1    | 1    | 0    | 1    | 1    | 1    | 1    | 1.44000     | EF  |
| 1    | 1    | 1    | 1    | 0    | 0    | 0    | 0    | 1.44500     | F0  |
| 1    | 1    | 1    | 1    | 0    | 0    | 0    | 1    | 1.45000     | F1  |
| 1    | 1    | 1    | 1    | 0    | 0    | 1    | 0    | 1.45500     | F2  |
| 1    | 1    | 1    | 1    | 0    | 0    | 1    | 1    | 1.46000     | F3  |
| 1    | 1    | 1    | 1    | 0    | 1    | 0    | 0    | 1.46500     | F4  |
| 1    | 1    | 1    | 1    | 0    | 1    | 0    | 1    | 1.47000     | F5  |
| 1    | 1    | 1    | 1    | 0    | 1    | 1    | 0    | 1.47500     | F6  |
| 1    | 1    | 1    | 1    | 0    | 1    | 1    | 1    | 1.48000     | F7  |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 0    | 1.48500     | F8  |
| 1    | 1    | 1    | 1    | 1    | 0    | 0    | 1    | 1.49000     | F9  |
| 1    | 1    | 1    | 1    | 1    | 0    | 1    | 0    | 1.49500     | FA  |
| 1    | 1    | 1    | 1    | 1    | 0    | 1    | 1    | 1.50000     | FB  |
| 1    | 1    | 1    | 1    | 1    | 1    | 0    | 0    | 1.50500     | FC  |
| 1    | 1    | 1    | 1    | 1    | 1    | 0    | 1    | 1.51000     | FD  |
| 1    | 1    | 1    | 1    | 1    | 1    | 1    | 0    | 1.51500     | FE  |
| 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1.52000     | FF  |

## Start Up Timing Diagram



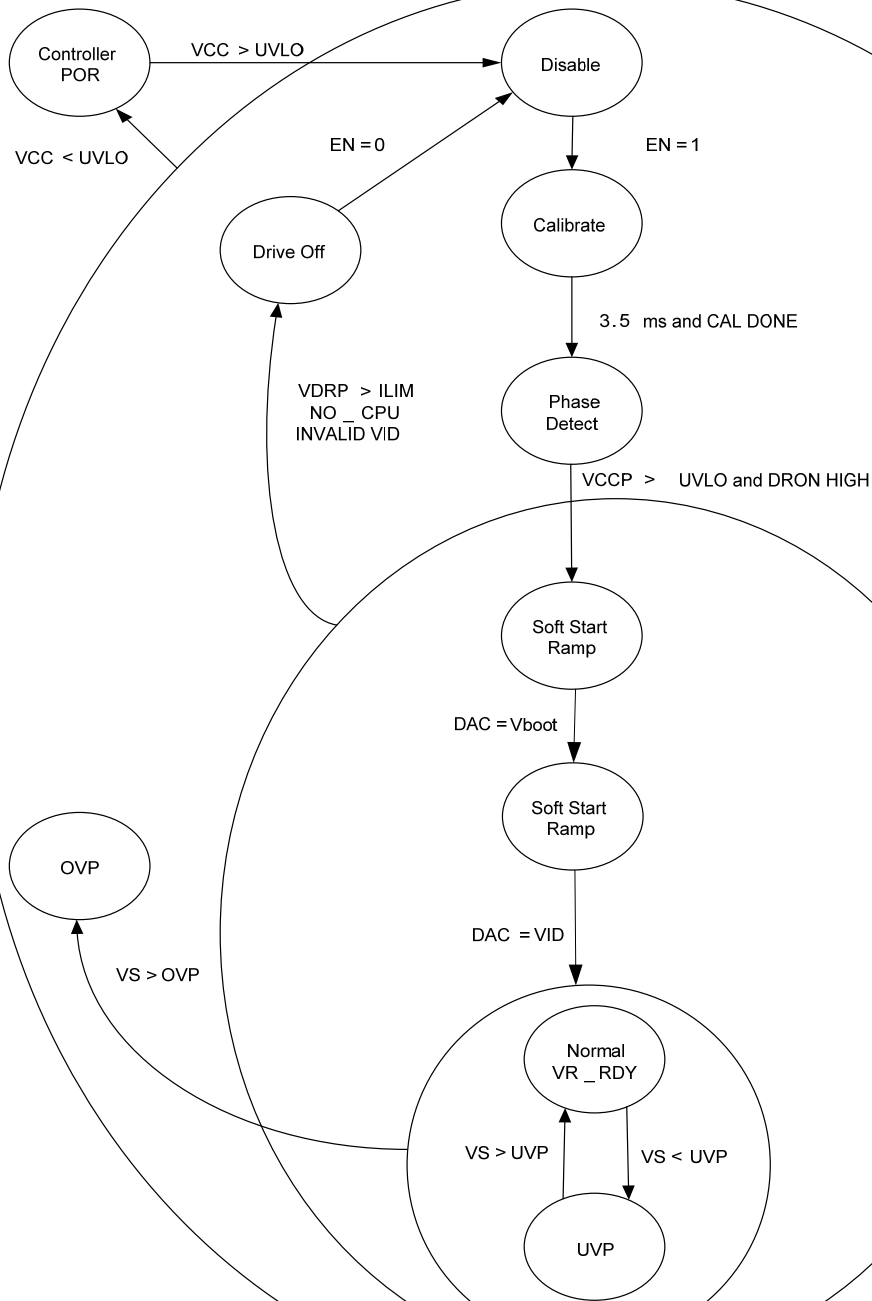
## SVID Timing Diagram



### State Truth Table

| STATE                                                                             | VR_RDY(A)<br>Pin | Error AMP<br>Comp(A) Pin | OVP(A)<br>& UVP(A)   | DRVON<br>PIN                         | Method of<br>Reset                         |
|-----------------------------------------------------------------------------------|------------------|--------------------------|----------------------|--------------------------------------|--------------------------------------------|
| <b>POR</b><br>0<VCC<UVLO                                                          | N/A              | N/A                      | N/A                  | Resistive pull<br>down               |                                            |
| <b>Disabled</b><br>EN < threshold<br>UVLO > threshold                             | Low              | Low                      | Disabled             | Low                                  |                                            |
| <b>Start up Delay &amp;<br/>Calibration</b><br>EN > threshold<br>UVLO > threshold | Low              | Low                      | Disabled             | Low                                  |                                            |
| <b>DRVON Fault</b><br>EN > threshold<br>UVLO > threshold<br>DRVON < threshold     | Low              | Low                      | Disabled             | Resistive pull up                    | Driver must<br>release<br>DRVON to<br>high |
| <b>Soft Start</b><br>EN > threshold<br>UVLO > threshold<br>DRVON > High           | Low              | Operational              | Active /<br>No latch | High                                 |                                            |
| <b>Normal Operation</b><br>EN > threshold<br>UVLO > threshold<br>DRVON > High     | High             | Operational              | Active /<br>Latching | High                                 | N/A                                        |
| <b>Over Voltage</b>                                                               | Low              | N/A                      | DAC+150mV            | High                                 |                                            |
| <b>Over Current</b>                                                               | Low              | Operational              | Last DAC<br>Code     | Low                                  |                                            |
| <b>VID Code = 00h</b>                                                             | Low              | Low                      | Disabled             | High,<br>PWM outputs in<br>mid state | Set Valid VID<br>Code                      |

## State Diagram



## General

The NCP6151S/NCP631S is a dual output four/three phase plus one phase dual edge modulated multiphase PWM controller designed to meet the Intel VR12 specifications with a serial SVID control interface. The NCP6151S/NCP631S implements PS0, PS1, and PS2 power saving states. It is designed to work in notebook, desktop, and server applications.

## Serial VID

The NCP6151S/NCP631S supports the Intel serial VID interface. It communicates with the microprocessor through three wires (SCLK, SDIO, ALERT#). The table of supported registers is shown below.

| Index | Name               | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Access | Default |
|-------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---------|
| 00h   | Vendor ID          | Uniquely identifies the VR vendor. The vendor ID assigned by Intel to ON Semiconductor is 0x1Ah                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | R      | 0x1Ah   |
| 01h   | Product ID         | Uniquely identifies the VR product. The VR vendor assigns this number.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | R      | 0x00    |
| 02h   | Product Revision   | Uniquely identifies the revision or stepping of the VR control IC. The VR vendor assigns this data.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | R      | 0x03    |
| 05h   | Protocol ID        | Identifies the SVID Protocol the NCP6151S supports                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | R      | 0x01    |
| 06h   | Capability         | <p>Informs the Master of the NCP6151S's Capabilities, 1 = supported, 0 = not supported</p> <p>Bit 7 = iout_format. Bit 7 = 0 when 1A = 1LSB of Reg 15h. Bit 7 = 1 when Reg 15 FFh = Icc_Max. Default = 1</p> <p>Bit 6 = ADC Measurement of Temp Supported = 1</p> <p>Bit 5 = ADC Measurement of Pin Supported = 0</p> <p>Bit 4 = ADC Measurement of Vin Supported = 0</p> <p>Bit 3 = ADC Measurement of Iin Supported = 0</p> <p>Bit 2 = ADC Measurement of Pout Supported = 1</p> <p>Bit 1 = ADC Measurement of Vout Supported = 1</p> <p>Bit 0 = ADC Measurement of Iout Supported = 1</p> | R      | 0xC7    |
| 10h   | Status_1           | Data register read after the ALERT# signal is asserted. Conveying the status of the VR.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | R      | 00h     |
| 11h   | Status_2           | Data register showing optional status_2 data.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | R      | 00h     |
| 12h   | Temp zone          | Data register showing temperature zones the system is operating in                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | R      | 00h     |
| 15h   | I_out              | 8 bit binary word ADC of current. This register reads 0xFF when the output current is at Icc_Max                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | R      | 01h     |
| 16h   | V_out              | 8 bit binary word ADC of output voltage, measured between VSP and VSN. LSB size is 8mV                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | R      | 01h     |
| 17h   | VR_Temp            | 8 bit binary word ADC of voltage. Binary format in deg C, IE 100C=64h. A value of 00h indicates this function is not supported                                                                                                                                                                                                                                                                                                                                                                                                                                                               | R      | 01h     |
| 18h   | P_out              | 8 bit binary word representative of output power. The output voltage is multiplied by the output current value and the result is stored in this register. A value of 00h indicates this function is not supported                                                                                                                                                                                                                                                                                                                                                                            | R      | 01h     |
| 1Ch   | Status 2 Last read | When the status 2 register is read its contents are copied into this register. The format is the same as the Status 2 Register.                                                                                                                                                                                                                                                                                                                                                                                                                                                              | R      | 00h     |
| 21h   | Icc_Max            | Data register containing the Icc_Max the platform supports. The value is measured on the ICCMAX pin on power up and placed in this register. From that point on the register is read only.                                                                                                                                                                                                                                                                                                                                                                                                   | R      | 00h     |
| 22h   | Temp_Max           | Data register containing the max temperature the platform supports and the level VR_hot asserts. This value defaults to 100°C and programmable over the                                                                                                                                                                                                                                                                                                                                                                                                                                      | R/W    | 64h     |

|     |                |                                                                                                                                                                                                                                                                                                                                                                                                                                   |    |     |
|-----|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|-----|
|     |                | SVID Interface                                                                                                                                                                                                                                                                                                                                                                                                                    |    |     |
| 24h | SR_fast        | Slew Rate for SetVID_fast commands. Binary format in mV/us.                                                                                                                                                                                                                                                                                                                                                                       | R  | 0Ah |
| 25h | SR_slow        | Slew Rate for SetVID_slow commands. It is 4X slower than the SR_fast rate. Binary format in mV/us                                                                                                                                                                                                                                                                                                                                 | R  | 02h |
| 26h | Vboot          | The Vboot is programmed using resistors on the Vboot pin which is sensed on power up. The NCP6151S will ramp to Vboot and hold at Vboot until it receives a new SVID SetVID command to move to a different voltage. Default value=0, i.e. this occurs if no resistor is connected to the Vboot pin. IN this case the NCP6151S will wait till it gets an SVID command to set the output voltage., VR12 VID format, IE 97h=1.0Volts | R  | 00h |
| 30h | Vout_Max       | Programmed by master and sets the maximum VID the VR will support. If a higher VID code is received, the VR should respond with "not supported" acknowledge. VR 12 VID format.                                                                                                                                                                                                                                                    | RW | FBh |
| 31h | VID setting    | Data register containing currently programmed VID voltage. VID data format.                                                                                                                                                                                                                                                                                                                                                       | RW | 00h |
| 32h | Pwr State      | Register containing the current programmed power state.                                                                                                                                                                                                                                                                                                                                                                           | RW | 00h |
| 33h | Offset         | Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is sign bit, 0=positive margin, 1= negative margin. Remaining 7 BITS are # VID steps for margin 2s complement.<br>00h=no margin<br>01h=+1 VID step<br>02h=+2 VID steps<br>FFh=-1 VID step<br>FEh=-2 VID steps.                                                                                                                                     | RW | 00h |
| 34h | MultiVR Config |                                                                                                                                                                                                                                                                                                                                                                                                                                   |    |     |

## BOOT VOLTAGE PROGRAMMING

The NCP6151S/NCP6131S has a Vboot voltage register that can be externally programmed for each output. The VBOOT also provides a feature that allows the "+1" single phase output to be disabled and effectively removed from the SVID bus. If the single phase output is disabled it alters the SVID address setting table to allow the multi-phase rail to show up at an even or odd address. See the Boot Voltage Table below.

**Boot Voltage Table**

| Boot Voltage (V) | Resistor Value (Ohms) |
|------------------|-----------------------|
| 0                | 10k                   |
| 0.85             | 25k                   |
| 0.9              | 45k                   |
| 0.95             | 70k                   |
| 1.0              | 95k                   |
| 1.1              | 125k                  |
| 1.5              | 165k                  |

|     |                        |
|-----|------------------------|
| VCC | Shutdown (VbootA only) |
|-----|------------------------|

## ADDRESSING THE NCP6151S/NCP6131S

The NCP6151S/NCP6131S supports 7 possible dual SVID device addresses and 8 possible single device addresses. Pin 32 (PWM1/ADDR) is used to set the SVID address. On power up a 10uA current is sourced from this pin through a resistor connected to this pin and the resulting voltage is measured. The two tables below provide the resistor values for each corresponding SVID address. For dual addressing follow the Dual SVID Address Table. The address value is latched at startup. If VBOOTA is pulled to VCC the aux rail will be removed from the SVID bus, the address will then follow the Single Address SVID table below.

**Dual SVID Address Table**

| Resistor Value | Main Rail SVID Address | Aux Rail SVID Address |
|----------------|------------------------|-----------------------|
| 10k            | 0000                   | 0001                  |
| 25k            | 0010                   | 0011                  |
| 45k            | 0100                   | 0101                  |
| 70k            | 0110                   | 0111                  |
| 95k            | 1000                   | 1001                  |
| 125k           | 1010                   | 1011                  |
| 165k           | 1100                   | 1101                  |

**Single SVID Address Table**

| Resistor Value | Main Rail SVID Address (VBOOTA tied to VCC) |
|----------------|---------------------------------------------|
| 10k            | 0000                                        |
| 22k            | 0001                                        |
| 36k            | 0010                                        |
| 51k            | 0011                                        |
| 68k            | 0100                                        |
| 91k            | 0101                                        |
| 120k           | 0110                                        |
| 160k           | 0111                                        |
| 220k           | 1000                                        |

## Remote Sense Amplifier

A high performance high input impedance true differential amplifier is provided to accurately sense the output voltage of the regulator. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage to

$$V_{DIFOUT} = (V_{VSP} - V_{VSN}) + (1.3V - V_{DAC}) + (V_{DROOP} - V_{CSREF})$$

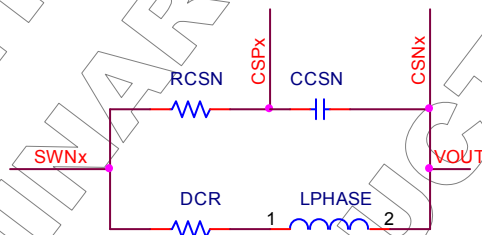
This signal then goes through a standard error compensation network and into the inverting input of the error amplifier. The non-inverting input of the error amplifier is connected to the same 1.3 V reference used for the differential sense amplifier output bias.

## High Performance Voltage Error Amplifier

A high performance error amplifier is provided for high bandwidth transient performance. A standard type 3 compensation circuit is normally used to compensate the system.

### Differential Current Feedback Amplifiers

Each phase has a low offset differential amplifier to sense that phase current for current balance and per phase OCP protection during soft-start. The inputs to the CSNx and CSPx pins are high impedance inputs. It is recommended that any external filter resistor RCSN not exceed 10kOhm to avoid offset issues with leakage current. It is also recommended that the voltage sense element be no less than 0.5mOhm for accurate current balance. Fine tuning of this time constant is generally not required.

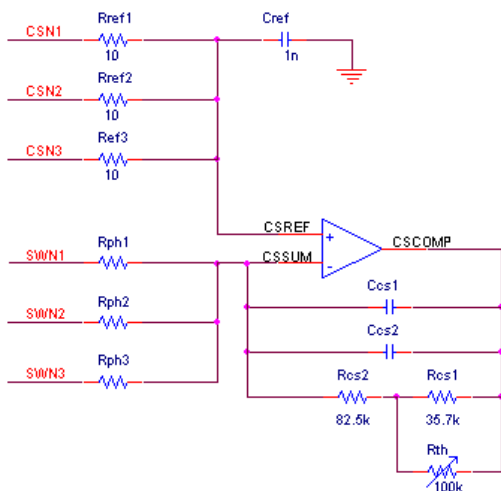


$$R_{CSN} = \frac{L_{PHASE}}{C_{CSN} * DCR}$$

The individual phase current is summed into the PWM comparator feedback in this way current is balanced via a current mode control approach.

### Total Current Sense Amplifier

The NCP6151S uses a patented approach to sum the phase currents into a single temperature compensated total current signal. This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The total current signal is floating with respect to CSREF. The current signal is the difference between CSCOMP and CSREF. The Ref(n) resistors sum the signals from the output side of the inductors to create a low impedance virtual ground. The amplifier actively filters and gains up the voltage applied across the inductors to recover the voltage drop across the inductor series resistance (DCR). Rth is placed near an inductor to sense the temperature of the inductor. This allows the filter time constant and gain to be a function of the Rth NTC resistor and compensate for the change in the DCR with temperature.



The DC gain equation for the current sensing:

$$V_{CSCOMP-CSREF} = - \frac{R_{cs2} + \frac{R_{cs1} * R_{th}}{R_{cs1} + R_{th}}}{R_{ph}} * (I_{out\_Total} * DCR)$$

Set the gain by adjusting the value of the R<sub>ph</sub> resistors. The DC gain should set to the output voltage droop. If the voltage from CSCOMP to CSREF is less than 100mV at ICCMAX then it is recommend to increase the gain of the CSCOMP amp and add a resistor divider to the Droop pin filter. This is required to provide a good current signal to offset voltage ratio for the ILIMIT pin. When no droop is needed, the gain of the amplifier should be set to provide ~100mV across the current limit programming resistor at full load. The values of R<sub>cs1</sub> and R<sub>cs2</sub> are set based on the 100k NTC and the temperature effect of the inductor and should not need to be changed. The NTC should be placed near the closest inductor. The output voltage droop should be set with the droop filter divider.

The pole frequency in the CSCOMP filter should be set equal to the zero from the output inductor. This allows the circuit to recover the inductor DCR voltage drop current signal. C<sub>cs1</sub> and C<sub>cs2</sub> are in parallel to allow for fine tuning of the time constant using commonly available values. It is best to fine tune this filter during transient testing.

$$F_z = \frac{DCR @ 25C}{2 * PI * L_{Phase}}$$

$$F_p = \frac{1}{2 * PI * \left( R_{cs2} + \frac{R_{cs1} * R_{th} @ 25C}{R_{cs1} + R_{th} @ 25C} \right) * (C_{cs1} + C_{cs2})}$$

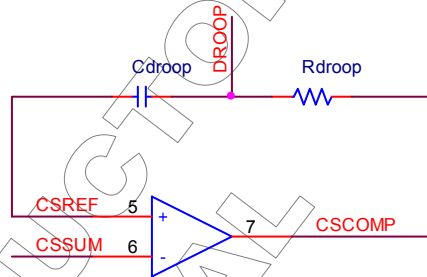
### Programming the Current Limit

The current limit thresholds are programmed with a resistor between the ILIMIT and CSCOMP pins. The ILIMIT pin mirrors the voltage at the CSREF pin and mirrors the sink current internally to IOUT (reduced by the IOUT Current Gain) and the current limit comparators. The 100% current limit trips if the ILIMIT sink current exceeds 10uA for 50us. The 150% current limit trips with minimal delay if the ILIMIT sink current exceeds 15uA. Set the value of the current limit resistor based on the CSCOMP-CSREF voltage as shown below.

$$R_{LIMIT} = \frac{R_{cs2} + \frac{R_{cs1} * R_{th}}{R_{cs1} + R_{th}} * (I_{out\_LIMIT} * DCR)}{10u} \quad \text{or} \quad R_{LIMIT} = \frac{V_{CSCOMP-CSREF @ ILIMIT}}{10u}$$

### Programming DROOP and DAC Feed-Forward Filter

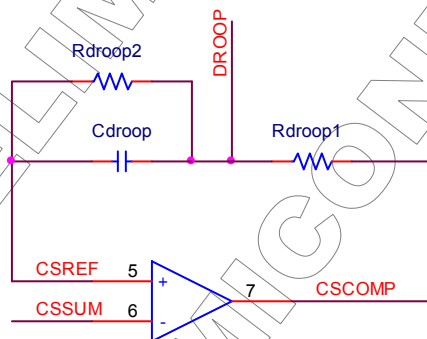
The signals DROOP and CSREF are differentially summed with the output voltage feedback to add precision voltage droop to the output voltage. The total current feedback should be filtered before it is applied to the DROOP pin. This filter impedance provides DAC feed-forward during dynamic VID changes. Programming this filter can be made simpler if CSCOMP-CSREF is equal to the droop voltage. Rd<sub>roop</sub> sets the gain of the DAC feed-forward and Cd<sub>roop</sub> provides the time constant to cancel the time constant of the system per the following equations. Cout is the total output capacitance and Rout is the output impedance of the system.



$$R_{droop} = C_{out} * R_{out} * 453.6 \times 10^6$$

$$C_{droop} = \frac{R_{out} * C_{out}}{R_{droop}}$$

If the Droop at maximum load is less than 100mV at ICCMAX we recommend altering this filter into a voltage divider such that a larger signal can be provided to the I<sub>LIMIT</sub> resistor by increasing the CSCOMP amp gain for better current monitor accuracy. The DROOP pin divider gain should be set to provide a voltage from DROOP to CSREF equal to the amount of voltage droop desired in the output. A current is applied to the DROOP pin during dynamic VID. In this case R<sub>droop1</sub> in parallel with R<sub>droop2</sub> should be equal to R<sub>droop</sub>



### Programming IOUT

The IOUT pin sources a current equal to the I<sub>LIMIT</sub> sink current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2V signal on IOUT. A pull-up resistor from 5V VCC can be used to offset the IOUT signal positive if needed.

$$R_{IOUT} = \frac{2.0V * R_{LIMIT}}{10 * \frac{R_{cs1} + R_{th}}{R_{ph}} * (I_{out\_ICC\_MAX} * DCR)}$$

### Programming ICC\_MAX and ICC\_MAXA

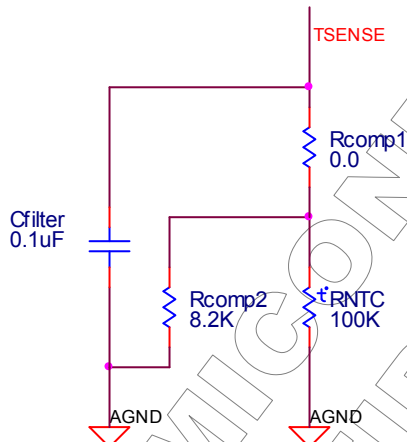
The SVID interface provides the platform ICC\_MAX value at register 21h for both the multiphase and the single phase rail. A resistor to ground on the IMAX and IMAXA pins program these registers at the time the part is enabled. 10uA is sourced from these pins to generate a voltage on the program resistor. The value of the register is 1A per LSB and is set by the equation below. The resistor value should be no less than 10k.

$$ICC\_MAX_{21h} = \frac{R * 10\mu A * 256A}{2V}$$

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## Programming TSENSE and TSENSEA

Two temperature sense inputs are provided. A precision current is sourced out the output of the TSENSE and TSENSEA pins to generate a voltage on the temperature sense network. The voltages on the temperature sense inputs are sampled by the internal A/D converter. A 100k NTC similar to the VISHAY ERT-J1VS104JA should be used. Rcomp1 is mainly used for noise. See the specification table for the thermal sensing voltage thresholds and source current.



## Precision Oscillator

A programmable precision oscillator is provided. The clock oscillator serves as the master clock to the ramp generator circuit. This oscillator is programmed by a resistor to ground on the ROSC pin. The oscillator frequency range is between 100KHz/phase to 1MHz/phase. The ROSC pin provides approximately 2V out and the source current is mirrored into the internal ramp oscillator. The oscillator frequency is approximately proportional to the current flowing in the ROSC resistor.

$$\frac{6.98k\Omega \times 440kHz}{F_s} = R_{osc}$$

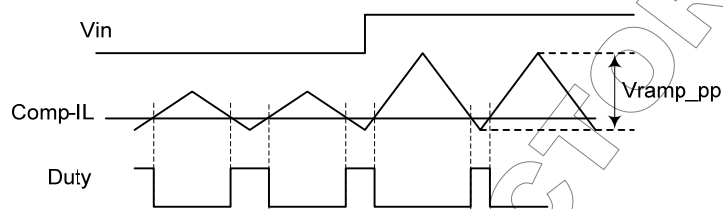
The oscillator generates triangle ramps that are 0.5~2.5 V in amplitude depending on the VRMP pin voltage to provide input voltage feed forward compensation. The ramps are equally spaced out of phase with respect to each other and the signal phase rail is set half way between phases 1 and 2 of the multi phase rail for minimum input ripple current.

## Programming the Ramp Feed-Forward Circuit

The ramp generator circuit provides the ramp used by the PWM comparators. The ramp generator provides voltage feed-forward control by varying the ramp magnitude with respect to the VRMP pin voltage. The VRMP pin also has a 4V UVLO function. The VRMP UVLO is only active after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled.

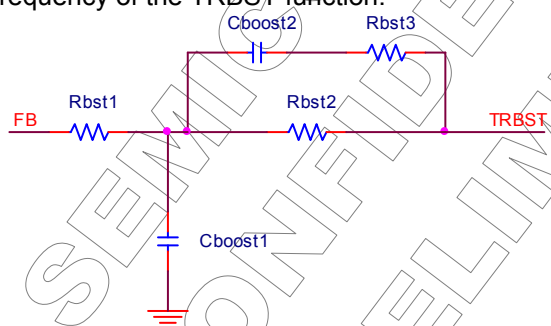
The PWM ramp time is changed according to the following,

$$V_{RAMPpk-pk_{pp}} = 0.1 * V_{VRMP}$$



### Programming TRBST

The TRBST pin provides a signal to offset the output after load release overshoot. This network should be fine tuned during the board tuning process and is only necessary in systems with significant load release overshoot. The TRBST network allows maximum boost for low frequency load release events to minimize load release undershoot. The network time constants are set up to provide a TRBST roll off at higher frequencies where it is not needed.  $C_{boost1} \cdot R_{bst1}$  controls the time constant of the load release boost. This should be set to counter the under shoot after load release.  $R_{bst1} + R_{bst2}$  controls the maximum amount of boost during rapid step loading.  $R_{bst2}$  is generally much larger than  $R_{bst1}$ . The  $C_{boost2} \cdot R_{bst2}$  time constant controls the roll off frequency of the TRBST function.



### PWM Comparators

During steady state operation, the duty cycle is centered on the valley of the triangle ramp waveform and both edges of the PWM signal are modulated. During a transient event the duty will increase rapidly and proportionally turning on all phases as the error amp signal increases with respect to the ramps to provide a highly linear and proportional response to the step load.

### PHASE DETECTION SEQUENCE

During start-up, the number of operational phases and their phase relationship is determined by the internal circuitry monitoring the PWM outputs. Normally, NCP6151S operates as a 4-phase V<sub>CORE</sub>+1-phase V<sub>AUX</sub> PWM controller, NCP6131S operates as a 3-phase V<sub>CORE</sub>+1-phase V<sub>AUX</sub> PWM controller. For NCP6151S, Connecting PWM4 pin to VCC programs 3-phase operation; While for NCP6131S, Connecting PWM2 pin to VCC programs 2-phase operation.

Prior to soft start, while ENABLE is high, NCP6151S PWM4 pin (or NCP6131S PWM2 pin) sinks approximately 100  $\mu$ A. An internal comparator checks the voltage of PWM4 pin (or PWM2 pin) and compares it to a threshold of hold of 2.5V. If the pin is tied to VCC, its voltage is above the threshold and the controller is configured to three phase operation otherwise the part operates in four phase mode.

The Aux rail can be disabled by pulling the VBOOT<sub>A</sub> signal to VCC. This changes the SVID address scheme to allow the multiphase to be programmed to any SVID Address odd or even. See the register resistor programming table.

## Phase Count Table

### NCP6151S

| Number of phases | Resistor Programming                 |
|------------------|--------------------------------------|
| 4+1              | PWM4 floating, VbootA programmed     |
| 3+1              | PWM4 tied to VCC, VbootA programmed  |
| 4+0              | PWM4 floating, VbootA tied to VCC    |
| 3+0              | PWM4 tied to VCC, VbootA tied to VCC |

### 3+1 Unused Pin Connection Table

| Unused Pin | Connect to |
|------------|------------|
| PWM4       | VCC        |
| CSN4       | GND        |
| CSP4       | GND        |

### 4+0 Unused Pin Connection Table

| Unused Pin | Connect to |
|------------|------------|
| VBOOTA     | VCC        |
| VSPA       | GND        |
| VSNA       | GND        |
| DIFFOUTA   | float      |
| FBA        | COMPA      |
| COMPA      | FBA        |
| TRBSTA     | float      |
| CSPA       | GND        |
| CSNA       | GND        |
| CSCOMP     | CSSUM      |
| CSSUM      | CSCOMP     |
| DROOPA     | GND        |
| ILIMA      | float      |
| TSENSEA    | GND        |
| PWMA       | float      |

### 3+0 Unused Pin Connection Table

| Unused Pin | Connect to |
|------------|------------|
| PWM4       | VCC        |
| CSN4       | GND        |
| CSP4       | GND        |

|          |        |
|----------|--------|
| VBOOTA   | VCC    |
| VSPA     | GND    |
| VSNA     | GND    |
| DIFFOUTA | float  |
| FBA      | COMPA  |
| COMPA    | FBA    |
| TRBSTA   | float  |
| CSPA     | GND    |
| CSNA     | GND    |
| CSCOMP   | CSSUM  |
| CSSUM    | CSCOMP |
| DROOPA   | GND    |
| ILIMA    | float  |
| TSENSEA  | GND    |
| PWMA     | float  |

### **NCP6131S**

| Number of phases | Resistor Programming                 |
|------------------|--------------------------------------|
| 3+1              | PWM2 floating, VbootA programmed     |
| 2+1              | PWM2 tied to VCC, VbootA programmed  |
| 3+0              | PWM2 floating, VbootA tied to VCC    |
| 2+0              | PWM2 tied to VCC, VbootA tied to VCC |

### **2+1 Unused Pin Connection Table**

| Unused Pin | Connect to |
|------------|------------|
| PWM2       | VCC        |
| CSN2       | GND        |
| CSP2       | GND        |

### **3+0 Unused Pin Connection Table**

| Unused Pin | Connect to |
|------------|------------|
| VBOOTA     | VCC        |
| VSPA       | GND        |
| VSNA       | GND        |
| DIFFOUTA   | float      |
| FBA        | COMPA      |
| COMPA      | FBA        |
| TRBSTA     | float      |
| CSPA       | GND        |
| CSNA       | GND        |
| CSCOMP     | CSSUM      |

|         |        |
|---------|--------|
| CSSUM   | CSCOMP |
| DROOPA  | GND    |
| ILIMA   | float  |
| TSENSEA | GND    |
| PWMA    | float  |

**2+0 Unused Pin Connection Table**

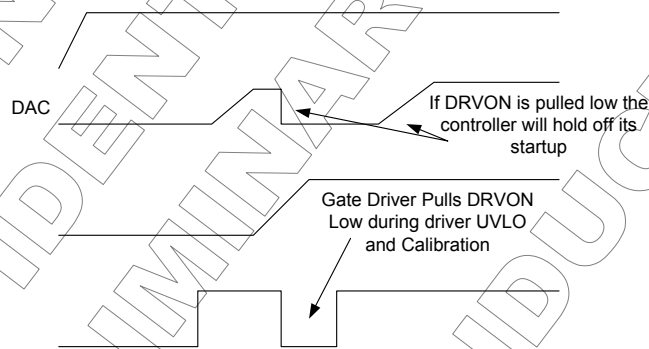
| Unused Pin | Connect to |
|------------|------------|
| PWM2       | VCC        |
| CSN2       | GND        |
| CSP2       | GND        |
| VBOOTA     | VCC        |
| VSPA       | GND        |
| VSNA       | GND        |
| DIFFOUTA   | float      |
| FBA        | COMP A     |
| COMP A     | FBA        |
| TRBSTA     | float      |
| CSPA       | GND        |
| CSNA       | GND        |
| CSCOMP     | CSSUM      |
| CSSUM      | CSCOMP     |
| DROOPA     | GND        |
| ILIMA      | float      |
| TSENSEA    | GND        |
| PWMA       | float      |

## Protection Features

### Input Under Voltage Protection

NCP6151S/NCP6131S monitors the 5V VCC supply and the VRMP pin for under voltage protection. The gate driver monitors both the gate driver VCC and the BST voltage (12V drivers only). When the voltage on the gate driver is insufficient it will pull DRVON low and notify the controller the power is not ready. The gate driver will hold DRVON low for a minimum period of time to allow the controller to restart its startup sequence. In this case the PWM is set back to the MID state and soft start would begin again. See the figure below.

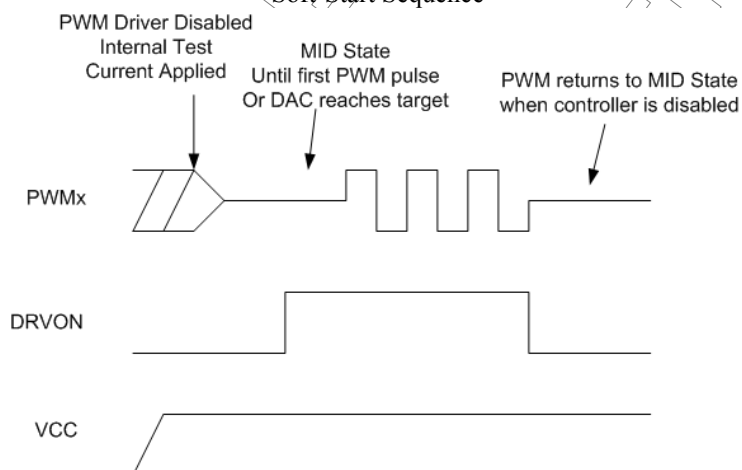
#### Gate Driver UVLO Restart



### Soft Start

Soft start is implemented internally. A digital counter steps the DAC up from zero to the target voltage based on the predetermined slew rate in the spec table. The PWM signals will start out open with a test current to collect data on phase count and for setting internal registers. After the configuration data is collected the controller enables and sets the PWM signal to the 2.0V MID state to indicate that the drivers should be in diode mode. DRVON will then be asserted and the COMP pin released to begin soft-start. The DAC will ramp from Zero to the target DAC codes and the PWM outputs will begin to fire. Each phase will move out of the MID state when the first PWM pulse is produced preventing the discharge of a pre-charged output.

#### Soft-Start Sequence



## Over Current Latch- Off Protection

The NCP6151S/NCP6131S provides two different types of current limit protection. During normal operation a programmable total current limit is provided that scales with the phase count during power saving operation. This limit is programmed with a resistor between the CSCOMP and ILIM pins. A second fixed per-phase current limit is provided for safe-start up monitoring during soft-start. The level of total current limit is set with the resistor from the ILIM pin to CSCOMP. The current through the external resistor connected between ILIM and CSCOMP is then compared to the internal current of 10uA and 15uA. If the current into the ILIM pin exceeds the 10A level an internal latch-off counter starts. The controller shuts down if the fault is not removed after 50us. If the current into the pin exceeds 15uA the controller will shut down immediately. To recover from an OCP fault the EN pin must be cycled low.

During startup the per phase current limit is active to protect the individual output stages. This limit monitors the voltage drop across the DCR through the CSPx and CSNx pins. The minimum threshold is:

The over-current limit is programmed by a resistor on the ILIM pin. The resistor value can be calculated by the following equation:

$$R_{ILIM} = \frac{V_{CSCOMP} - V_{CSREF}}{10\mu A}$$

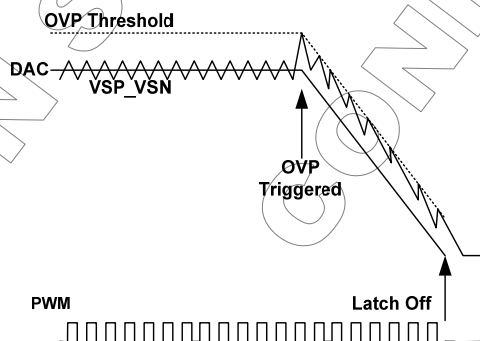
## Under Voltage Monitor

The output voltage is monitored at the output of the differential amplifier for UVLO. If the output falls more than 300mV below the DAC-DROOP voltage the UVLO comparator will trip sending the VR\_RDY signal low.

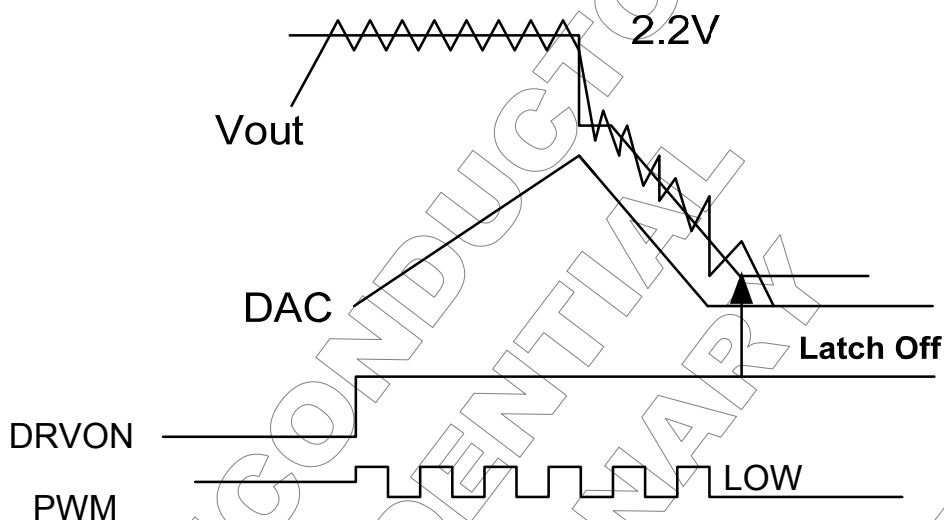
## Over Voltage Protection

During normal operation the output voltage is monitored at the differential inputs VSP and VSN. If the output voltage exceeds the DAC voltage by approximately 175 mV, PWMs will be forced low until the voltage drops below the OVP threshold after the first OVP trip the DAC will ramp down to zero to avoid a negative output voltage spike during shutdown. When the DAC gets to zero the PWMs will be forced low and the DRVON will remain high. To reset the part the Enable pin must be cycled low. During soft-start, the OVP threshold is set to 2.2V. This allows the controller to start up without false triggering the OVP. Prior to soft-start the gate drivers will provide OVP protection directly at the switching nodes.

### OVP Threshold Behavior



### Start up OVP Threshold Behavior



### Layout Notes

The NCP6151S/NCP6131S has differential voltage and current monitoring. This improves signal integrity and reduces noise issues related to layout for easy design use. To insure proper function there are some general rules to follow. Always place the inductor current sense RC filters as close to the CSN and CSP pins on the controller as possible. Place the VCC decoupling caps as close as possible to the controller VCC pin. The high frequency filter cap on CSREF and the 10 ohm CSREF resistors should be placed close to the controller. The small high feed back cap from COMP to FB should be as close to the controller as possible. Please minimize the capacitance to ground of the FB traces by keeping them short. The filter cap from CSCOMP to CSREF should also be close to the controller.

# QFN52 SINGLE ROW 6x6, 0.4P PACKAGE DIMENSIONS

Unit:

